Highly Versatile Buck-Boost Ambient Energy Manager Battery Charger For Up to 7-cell Solar Panels

Features

Ultra-low power start-up

- Cold start from 275 mV input voltage and 3 µW input power (typical)

Very efficient energy extraction

- Open-circuit voltage sensing for Maximum Power Point Tracking (MPPT)
- Selectable open-circuit voltage ratios from 60% to 90% or fixed impedance
- Programmable MPPT sensing period
- MPPT voltage operation range from 100 mV to 4.5 V

Adaptive and smart energy management

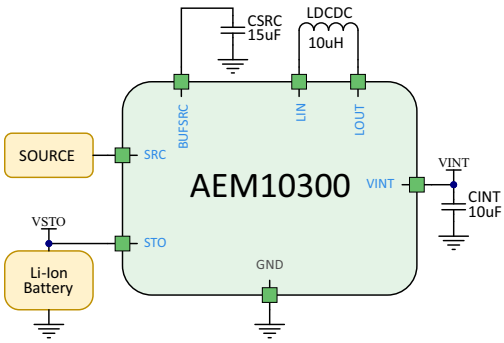
- Switches automatically between boost, buck-boost and buck operation, to maximize energy transfer from its input to the output

Battery protection features

- Selectable over-charge and over-discharge protection for any type of rechargeable battery or (super-)capacitor
- Fast super-capacitor charging
- Dual cell super-capacitor balancing circuit

Smallest footprint, smallest BOM

- Only three external components are required
- One 10 µH inductor
- Two capacitors: one 10 µF, one 15 µF



Description

The AEM10300 is an integrated energy management circuit that extracts DC power from an ambient energy harvesting source to store energy in a storage element. The AEM10300 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of applications.

Thanks to its Maximum Power Point Tracking system, the AEM10300 extracts the maximum energy available from the source. It integrates an ultra-low power DCDC converter which operates with input voltages ranging from 100 mV to 4.5 V.

With its unique cold start circuit, the AEM10300 can start harvesting with an input voltage as low as 275 mV and from an input power of 3 µW. The preset protection levels determine the storage element voltages protection thresholds to avoid over-charging and over-discharging the storage element and thus avoiding damaging it. Those are set through configuration pins. Moreover, special modes can be obtained at the expense of a few configuration resistors.

The chip integrates all active elements for powering a typical wireless sensor. Only two capacitors and one inductor are required.

Applications

- Asset Tracking/Monitoring
- Retail ESL/ Smart sensors
- Smart home/building
- Industrial applications
- Aftermarket automotive

Device Information

Part Number	Package	Body size [mm]
10AEM10300C0000	QFN 28-pin	4x4mm

Evaluation Board

Part Number
2AAEM10300C0010

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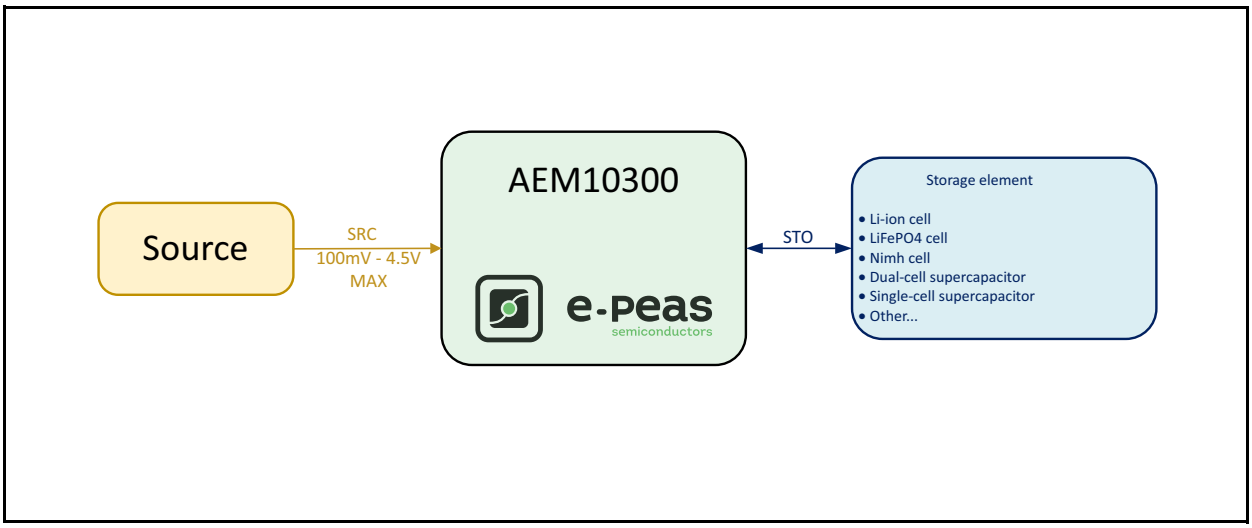


Figure 1: Simplified Schematic View

1. Introduction

The AEM10300 is a full-featured energy efficient power management circuit able to harvest energy from an energy source (connected to SRC) to charge a storage element (connected to STO). This is done with a minimal bill of material: only 2 capacitors and one inductor are needed for a basic setup.

The heart of the AEM10300 is a regulated switching DCDC converter with high power conversion efficiency.

At first start-up, as soon as a required cold start voltage of 275 mV and a sparse amount of power of at least 3 µW is available at the source, the AEM10300 cold starts. After the cold start, the AEM extracts the power available from the source if the working input voltage is at least 100 mV.

Through four configuration pins (STO_CFG[3:0]), the user can select a specific operating mode out of 15 modes that cover most application requirements without any dedicated external component. Those operating modes define the protection levels of the storage element. If none of those 15 modes fit the user's storage element, a custom mode is also available to allow the user to define a mode with custom specifications.

Status pin ST_STO provides information about the voltage levels of the storage element. ST_STO is asserted when the voltage of the storage element V_{STO} is above V_{CHRDY} and is reset when the voltage drops below V_{OVDIS}.

The Maximum Power Point (MPP) ratio is configurable thanks to three configuration pins (R_MPP[2:0]) and ensures an optimum biasing of the harvester to maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins (T_MPP[1:0]) that sets the periodicity and the duration of the MPP evaluation.

The AEM10300's DCDC converter can work in two modes: LOW POWER MODE and HIGH POWER MODE, each one of these being optimized for a power range on SRC.

The charging of the storage element can be prevented by pulling EN_STO_CH to GND, typically to protect the storage element if the temperature is too low/high to safely charge it.

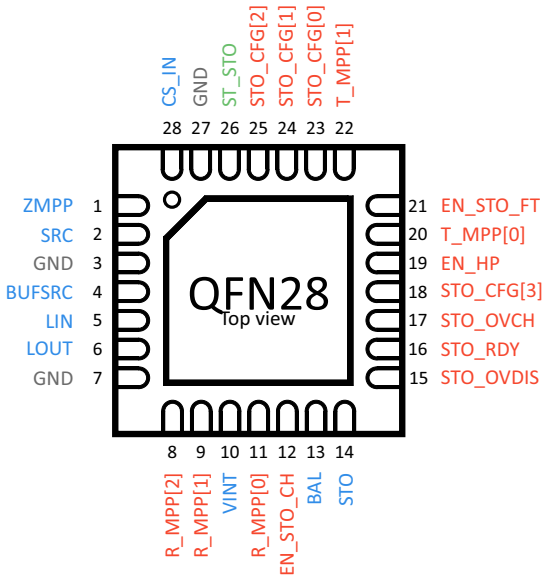


Figure 2: Pinout Diagram QFN 28-pin

NAME	PIN NUMBER	FUNCTION
Power pins		
ZMPP	1	Used for the configuration of the ZMPP (optional). Must be left floating if not used.
SRC	2	Connection to the harvested energy source.
BUFSRC	4	Connection to an external capacitor buffering the DCDC converter input.
LIN	5	DCDC inductance connection.
LOUT	6	DCDC inductance connection.
VINT	10	Internal voltage supply.
BAL	13	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.
STO	14	Connection to the energy storage element - battery or (super-)capacitor. Cannot be left floating. Must be connected to a minimum capacitance of 100 µF or to a rechargeable battery.
CS_IN	28	Input for the external cold start circuit.
Status pins		
ST_STO	26	Logic output. Asserted when the storage device voltage V_{STO} rises above the V_{CHRDY} threshold, reset when V_{STO} drops below the V_{OVDIS} threshold or when V_{SRC} isn't available. High level is V_{STO}.

Table 1: Power and Status Pins

NAME	PIN NUMBER	Function
Configuration pins		
R_MPP[2]	8	Used for the configuration of the MPP ratio.
R_MPP[1]	9	
R_MPP[0]	11	
T_MPP[0]	20	Used for the configuration of the MPP timings.
T_MPP[1]	22	
STO_CFG[0]	23	Used for the configuration of the threshold voltages for the energy storage element (V_{OVDIS}, V_{CHRDY} and V_{OVCH}).
STO_CFG[1]	24	
STO_CFG[2]	25	
STO_CFG[3]	18	
STO_OVCH	17	Used for the configuration of the threshold voltages (V_{OVDIS}, V_{CHRDY} and V_{OVCH}) for the energy storage element when STO_CFG[3:0] are set to custom mode (optional). Must be left floating if not used.
STO_OVDIS	15	
STO_RDY	16	
EN_STO_CH	12	- Pulled up to VINT: enables the charging of the battery - Pulled down to GND: disables the charging of the battery
EN_HP	19	- Pulled up to VINT: HIGH POWER MODE enabled - Pulled down to GND: HIGH POWER MODE disabled
Other		
GND	3, 7, 21 27	Ground connection, best possible connection to PCB ground plane.
	Exposed pad	

Table 2: Configuration and Ground Pins

2. Absolute Maximum Ratings

Parameter	Value
Voltage on STO, SRC, BUFSRC, LIN, LOUT, ZMPP, BAL, CS_IN	-0.3 V to 5.5 V
Voltage on VINT, T_MPP[1:0], R_MPP[2:0], STO_CFG[3:0], STO_OVCH, STO_OVDIS, STO_RDY, EN_HP, EN_STO_CH	-0.3 V to 2.75 V
Operating junction temperature	-40 °C to 125 °C
Storage temperature	-65 °C to 150 °C
ESD HBM voltage	> 2000 V
ESD CDM voltage	> 500 V

Table 3: Absolute Maximum Ratings

3. Thermal Resistance

Package	θJA	θJC	Unit
QFN 28-pin	TBD	TBD	°C/W

Table 4: Thermal Resistance

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper EESD precautions should be taken to avoid performance degradation or loss of functionality

Table 5: ESD Caution

4. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Source power required for cold start	V_{STO} > Vchrdy		3		µW
		V_{STO} < Vchrdy		6		µW
V_{SRC}	Input voltage of the energy source	During cold start		0.275	4.5	V
		After cold start	0.1		4.5	V
R_{ZMPP}	MPPT ratio	see Table 11	60, 65, 70, 75, 80, 85 or 90, depending on R_MPP[2:0] configuration			%
Timing						
$T_{MPP,EVAL}$	Duration of a MPP evaluation		50% of Table 11		200% of Table 11	ms
$T_{MPP,PERIOD}$	Time between two MPP evaluations		50% of Table 11		200% of Table 11	s
Storage element						
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging	see Table 9	Depends on STO_CFG[3:0] configuration			V
V_{CHRDY}	Minimum voltage required on the storage element before asserting the ST_STO					V
V_{OVDIS}	Minimum voltage accepted on the storage element before reseting ST_STO					V
Internal supply & Quiescent Current						
V_{VINT}	Internal voltage supply			2.2		V
I_Q	Quiescent current on STO	V_{STO} = 3.7V V_{LOAD} = 2.5V EN_SLEEP = 0 HP_EN = 0		5.9		nA
Symbol	**Logic Level**		**Low**		**High**	
Logic output pins						
ST_STO	Logic output levels on the status STO pins		GND		V_{STO}	

Table 6: Typical Electrical Characteristics

5. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External Components					
LDCDC	Inductor of the DCDC converter		10		µH
CSRC	Capacitor decoupling the SRC terminal	15			µF
CINT	Capacitor decoupling the VINT terminal	10			µF
CSTO	Optional - Capacitor on STO if no storage element is connected (see Section 8.8.1)	100			µF
STO_OVCH	Configuration of V_{OVCH} in custom mode	1	Section 0.9	100	MΩ
STO_OVDIS	Configuration of V_{OVDIS} in custom mode				
STO_RDY	Configuration of V_{CHRDY} in custom mode				
ZMPP	Optional - Used for the configuration of the ZMPP tracking function	10	Section 8.6	100K	Ω
Symbol	Logic Level	Low		High	
Logic input pins					
R_MPP[2:0]	Configuration pins for the MPP evaluation	GND		VINT	
T_MPP[1:0]	Configuration pins for the MPP timing	GND		VINT	
STO_CFG[3:0]	Configuration pins for the STO voltage	GND		VINT	
EN_STO_FT	Configuration pin for the controller	GND		VINT	
EN_STO_CH	Configuration pin for the controller	GND		VINT	
EN_HP	Configuration pin for the controller	GND		VINT	

Table 7: Recommended Operation Conditions

6. Functional Block Diagram

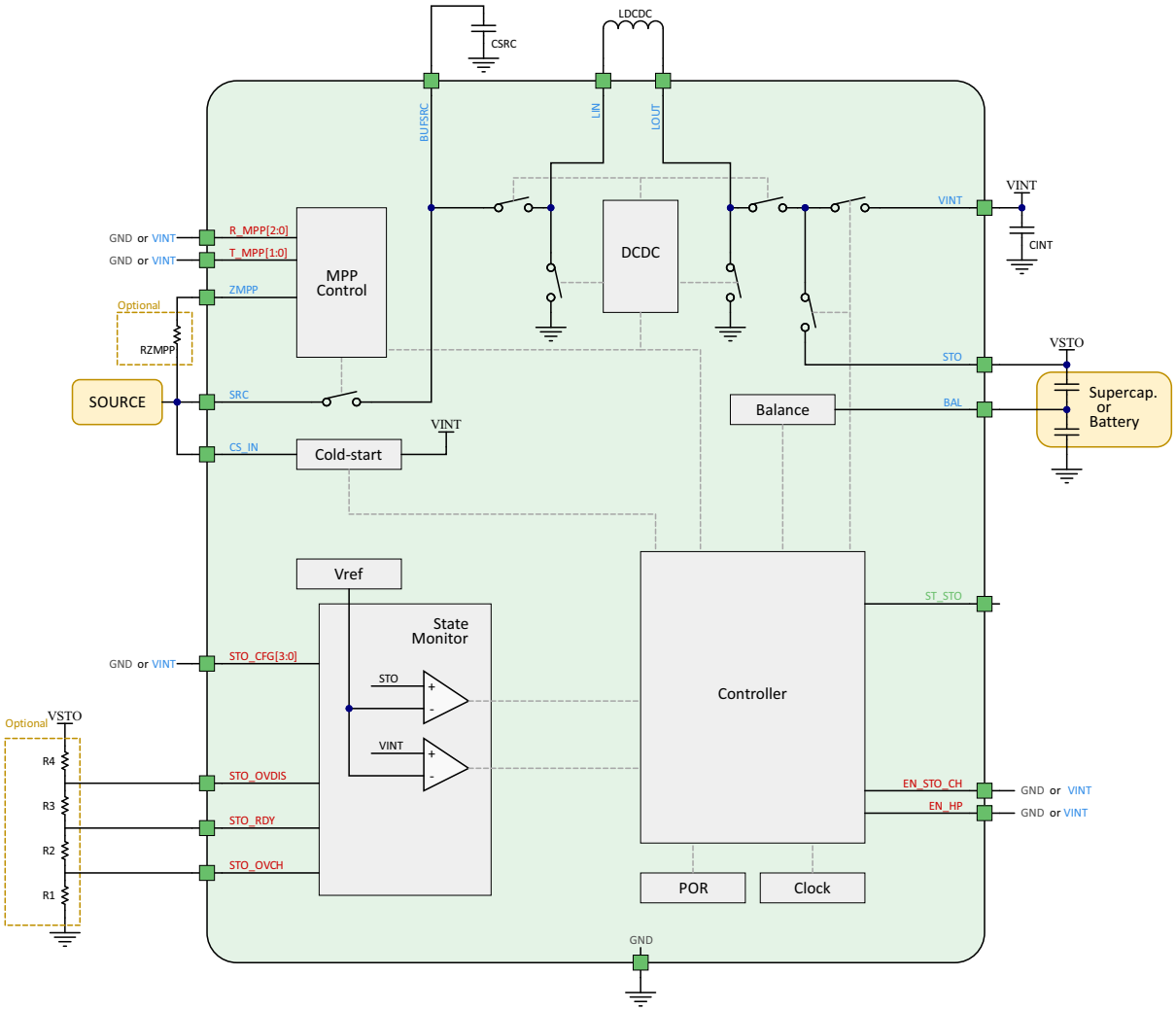


Figure 3: Functional Block Diagram

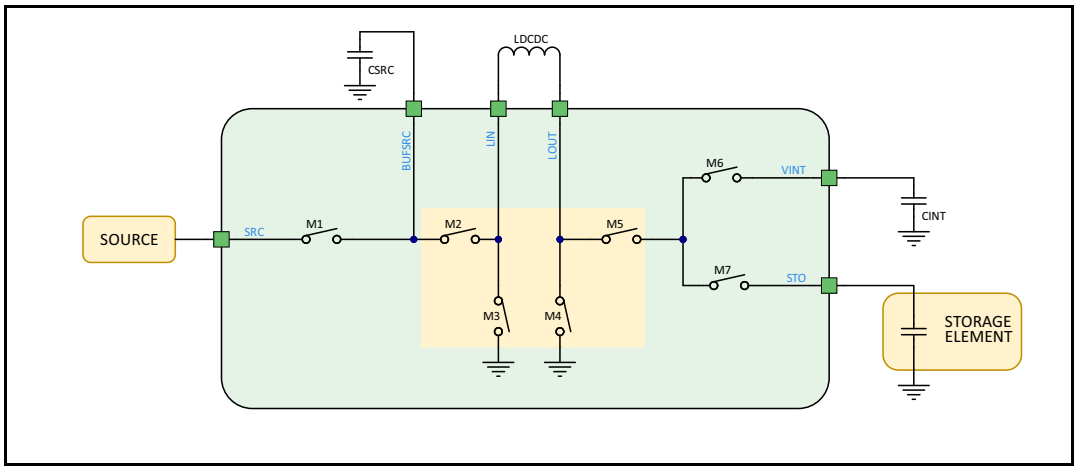


Figure 4: Simplified Schematic View of the AEM10300

7. Theory of Operation

7.1. DCDC Converter

The DCDC converter converts the voltage available at BUFSRC to a level suitable for charging the storage element STO or to regulatethe internal supply VINT. The switching transistors of the DCDC converter are M2, M3, M4 and M5. Thanks to M6 and M7, the controller selects between VINT and STO respectively as the converter output. STO is selected as an output only when VINT does not need to be supplied.

The reactive power component of this converter is the external inductor LDCDC. Periodically, the MPP control circuit disconnects the source from the BUFSRC pin with the transistor M1 in order to let the harvester on SRC rise to its open-circuit voltage V_{OC} and measure it. This is done to define the optimal voltage level V_{MPP}, which is determined by applying the MPP ratio on V_{OC}. BUFSRC is decoupled by the capacitor CSRC, which smooths the voltage against the current pulses pulled by the DCDC converter. The storage element is connected to the STO pin.

Depending on its input voltage and its output voltage, the DCDC converter will work as a boost converter, a buck converter or a buck-boost converter. The maximum power that can be harvested and supplied to the output depends on the power mode (HIGH POWER MODE or LOW POWER MODE), which is configured through the EN_HP pin (see Section 8.1).

DCDC converter mode	Input Voltage / Output Voltage
Boost	$V_{IN} < V_{OUT}$ - 250mV
Buck	$V_{IN} > V_{OUT}$ + 250 mV
Buck - Boost	V_{OUT} - 250mV < V_{IN} < V_{OUT} + 250mV

Table 8: DCDC Converter Modes

7.2. Reset and Wake Up States

The RESET STATE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 275 mV and a sparse amount of power of just 3 µW become available on CS_IN (usually connected to SRC), the AEM10300 switches to WAKE-UP STATE, and energy is extracted from SRC to make V_{VINT} rise to 2.2 V. When V_{VINT} reaches those 2.2 V, the AEM10300 switches to .

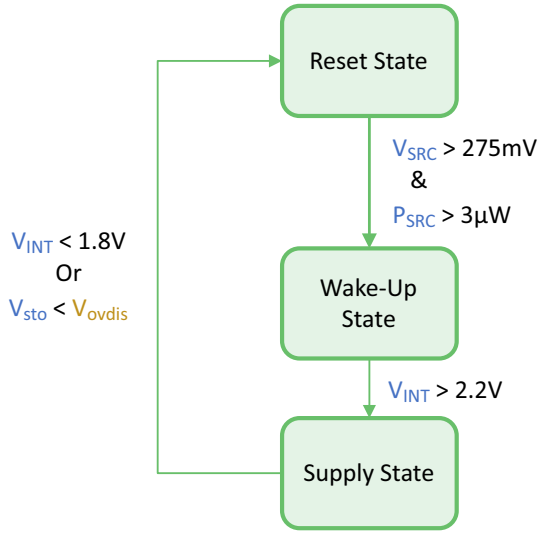


Figure 5: Diagram of the AEM10300 States

7.3. Supply State

In SUPPLY STATE, three scenarios are possible:

- There is enough power provided by the source (SRC) to keep V_{VINT} at 2.2 V. The excessive power is used to charge the storage element on STO. In that case, the circuit remains in SUPPLY STATE.If STO is fully charged, the DCDC converter is disabled to prevent over-charging the storage element.
- Due to a lack of power from the source, V_{STO} falls below V_{OVDIS}. In this case, the circuit enters RESET STATE as explained in Section 0.3.
- There is no power on SRC. It is therefore not possible to maintain VINT to 2.2 V. In this case, the circuit enters in RESET STATE.

From time to time, when VINT voltage falls below its regulation value, the DCDC converter switches its output to keep VINT voltage from SRC close to 2.2 V. If no power is available on SRC, VINT is not maintained.

7.4. Maximum Power Point Tracking

During SUPPLY STATE, the voltage on SRC is regulated by an internal Maximum Power Point Tracking (MPPT) module. The MPPT module evaluates V_{MPP}, the voltage at which the source provides the highest possible power, as a given fraction of the open-circuit voltage of the source V_{OC}. This ratio is set by the R_MPP[2:0] terminals according to Table 10. The sampling period and duration are set according to Table 11 by the T_MPP[1:0] terminals. The AEM10300 supports any V_{MPP} levels in the range from 100 mV to 4.5 V. It offers a choice of seven values for the V_{MPP} / V_{OC} fraction. It can also match the input impedance of the DCDC converter with an impedance connected to the ZMPP terminal as explain as explained in section 8.6.

7.5. Balancing for Dual-Cell Supercapacitor

The balancing circuit allows the user to balance the internal voltage of the dual-cell supercapacitor connected to STO in order to avoid damaging the supercapacitor because of excessive voltage on one cell.

If BAL is connected to GND, the balancing circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on STO.

If BAL is connected to the node between both cells of a supercapacitor, the balancing circuit compensates for any mismatch of the two cells that could lead to the over-charge of one of two cells. The balancing circuit ensures that BAL remains close to V_{STO} / 2. This configuration must be used if a dual-cell supercapacitor is connected to STO, and that this supercapacitor requires cells balancing.

8. System Configuration

8.1. High Power / Low Power Mode

When EN_HP is pulled to VINT, the DCDC converter is configured to HIGH POWER MODE. This allows higher currents to be extracted from the DCDC converter input (SRC) to the DCDC converter output (STO).

8.2. Storage Element Configuration

Through four configuration pins (STO_CFG[3:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 9. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling its charging.
- V_{CHRDY}: minimum voltage required on the storage element before asserting the ST_STO
- V_{OVDIS}: minimum voltage accepted on the storage element before resetting ST_STO.

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3]	STO_CFG[2]	STO_CFG[1]	STO_CFG[0]	V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
0	0	0	0	3.00 V	3.50 V	4.05 V	Li-ion battery
0	0	0	1	2.80 V	3.10 V	3.60 V	LiFePO4 battery
0	0	1	0	1.85 V	2.40 V	2.70 V	NiMH battery
0	0	1	1	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor
0	1	0	0	0.20V	1.00 V	2.60 V	Single-cell supercapacitor
0	1	0	1	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor
0	1	1	0	1.85 V	2.30 V	2.60 V	NGK
0	1	1	1	Custom Mode			
1	0	0	0	1.10 V	1.25 V	1.50 V	Ni-Cd 1 cells
1	0	0	1	2.20 V	2.50 V	3.00 V	Ni-Cd 2 cells
1	0	1	0	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor
1	0	1	1	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor
1	1	0	0	2.00 V	2.30 V	2.60 V	ITEN / Umal Murata
1	1	0	1	3.00 V	3.50 V	4.35 V	Li-Po battery
1	1	1	0	2.60 V	2.70 V	4.00 V	Tadiran TLI1020A
1	1	1	1	2.60 V	3.50 V	3.90 V	Tadiran HLC1020

Table 9: Storage Element Configuration Pins

8.3. Custom Mode Configuration

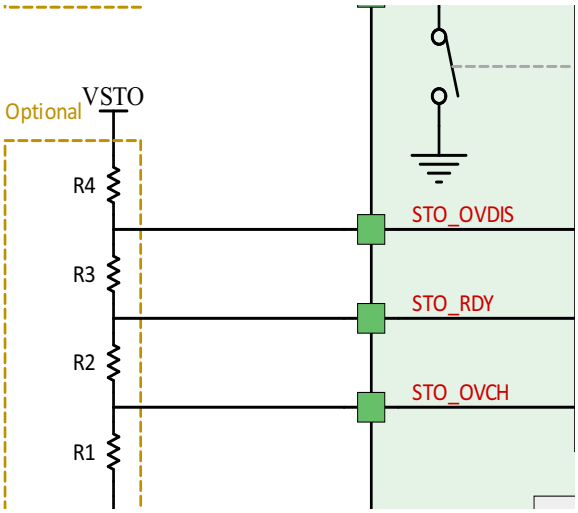


Figure 6: Custom Mode Settings

When STO_CFG[3:0] = 0111, the custom mode is selected and all four configuration resistors must be wired as shown in Figure 6.

V_{OVCH}, V_{CHRDY} and, V_{OVDIS} are defined thanks to R1, R2, R3 and R4, which can be determined within the following constraints:

- RT = R1 + R2 + R3 + R4
- 1 MΩ ≤ RT ≤ 100 MΩ
- R1 = RT (1 V / V_{OVCH})
- R2 = RT (1 V / V_{CHRDY} - 1 V / V_{OVCH})
- R3 = RT (1 V / V_{OVDIS} - 1 V / V_{CHRDY})
- R4 = RT (1 - 1 V / V_{OVDIS})

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be adhered to ensure the functionality of the chip:

- V_{CHRDY} + 0.05 V ≤ V_{OVCH} ≤ 4.5 V
- V_{OVDIS} + 0.05 V ≤ V_{CHRDY} ≤ V_{OVCH} - 0.05 V
- 1V ≤ V_{OVDIS}

8.4. Disable Storage Element Charging

Pulling down EN_STO_CH pin to GND disables the charging of the storage element connected to STO. This can be done for example to protect the storage element when the system detects that the environment temperature is too low or too high to safely charge the storage element.

While EN_STO_CH is pulled down, VINT can still be supplied from SRC.

To enable charging the storage element on STO, EN_STO_CH must be pulled up to VINT.

8.5. MPPT Configuration

There are two kinds of pins to configure the maximum point tracking. The first configuration pins allows for selecting the MPP tracking ratio based on the characteristic of the input power source. The configuration pins are R_MPP[2:0].

	Configuration pins		MPPT ratio
R_MPP[2]	R_MPP[1]	R_MPP[0]	V_{MPP} / V_{OC}
0	0	0	60%
0	0	1	65%
0	1	0	70%
0	1	1	75%
1	0	0	80%
1	0	1	85%
1	1	0	90%
1	1	1	ZMPP

Table 10: MPP Ratio Configuration Pins

The second kind of configuration pins allows for configuring the duration of an MPP evaluation and the time between two MPP evaluations. The configurations pins are T_MPP[1:0]

Configuration pins		MPPT timing	
T_MPP[1]	T_MPP[0]	Sampling duration	Sampling period
0	0	5.19 ms	280 ms
0	1	70.8 ms	4.5 s
1	0	280 ms	17.87 s
1	1	1.12 s	71.7 s

Table 11: MPP Timing Configuration Pins

8.6. ZMPP Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM10300 can regulate the input impedance of the DCDC converter so that it matches a constant impedance R_{ZMPP} connected to the ZMPP pin. In this case, the AEM10300 regulates V_{SRC} at a voltage that is the product of the ZMPP resistance R_{ZMPP} and the current available at the SRC input.

- 10 Ω ≤ R_{ZMPP} ≤ 100 KΩ

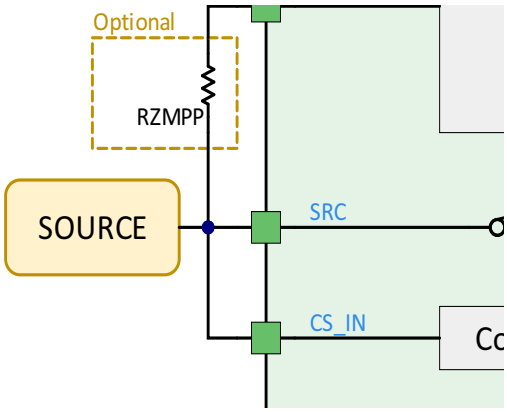


Figure 7: R_{ZMPP} Connection to the AEM10300

8.7. Source to Storage Element Feed-Through

When the harvester connected to SRC delivers a high amount of power, the AEM might not be able to pull enough current to regulate V_{SRC} to the MPP voltage. The voltage on SRC thus increases, eventually above 5V. To maximize the energy extracted in that case, the AEM30330 can be configured to create a direct feed-through current path from SRC to STO when V_{SRC} is above 5V. This is measured when the AEM is pulling current from the source (not during an MPP evaluation).

If the MPPT module detects that V_{SRC} is higher than 4 V and EN_STO_FT is set, the SRC is monitored. From that moment, if the AEM10300 detects that V_{SRC} rises above 5 V and if the storage element is not fully charged, the switch between the SRC and STO pins is closed until V_{SRC} drops below 5 V or until the storage element is fully charged.

This feature is enabled by pulling up EN_STO_FT pin to VINT. However, it is disabled if the storage element is fully charged, or when a MPP evaluation is occurring. Therefore the circuit must still be protected from any overshoot voltage on SRC above 5.5 V, for instance by a zener diode.

8.8. External Components

Refer to Figure 9 to have an illustration of the external components wiring.

8.8.1. Storage element information

The energy storage element of the AEM10300 can be a rechargeable battery, a supercapacitor or a capacitor. The size of the storage element must be determined so that its voltage does not fall below V_{OVDIS} even during current peaks pulled by the application. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to decouple the battery with a capacitor.

If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor CSTO of at least 100 µF connected between STO and GND. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the whole subsystem.

8.8.2. External inductor information

The AEM10300 operates with one standard miniature inductor. LDCDC must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favours the power conversion efficiency of the DCDC converter. The recommended value is 10 µH.

8.8.3. External capacitors information

CSRC

This capacitor acts as an energy buffer at the input of the DCDC converter. It prevents large voltage fluctuations when the DCDC converter is switching. The recommended value is 15 µF.

CINT

This capacitor acts as an energy buffer for the internal voltage supply. The recommended value is 10 µF.

9. Typical Application Circuits

9.1. Example Circuit 1

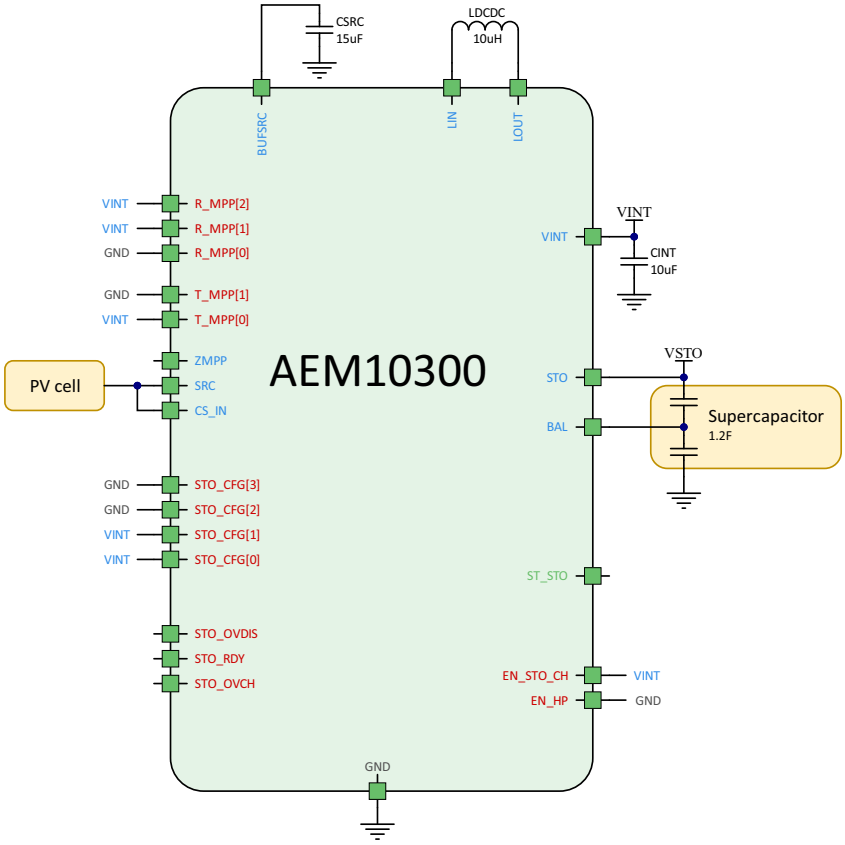


Figure 8: Typical Application Circuit 1

The circuit is an example of a system with solar energy harvesting. It uses a pre-defined operating mode that use standard components, and a supercapacitor as energy storage.

- Energy source: PV cell
- R_MPP[2:0] = 110: the MPP ratio is set to 90%
- T_MPP[1:0] = 01: the MPP sampling period is 4.5 s and the MPP sampling duration is 70.8 ms
- STO_CFG[3:0] = 0011: the storage element is a dual-cell supercapacitor, with:
  - V_{OVCH} = 4.65 V
  - V_{CHRDY} = 1.00 V
  - V_{OVDIS} = 0.20 V
- The balancing pin of the dual-cell supercapacitor is connected to BAL
- EN_STO_CH is connected to VINT: the charging of the storage element on STO is disabled
- EN_HP is connected to GND: the DCDC converter is in LOW POWER MODE

9.2. Example Circuit 2

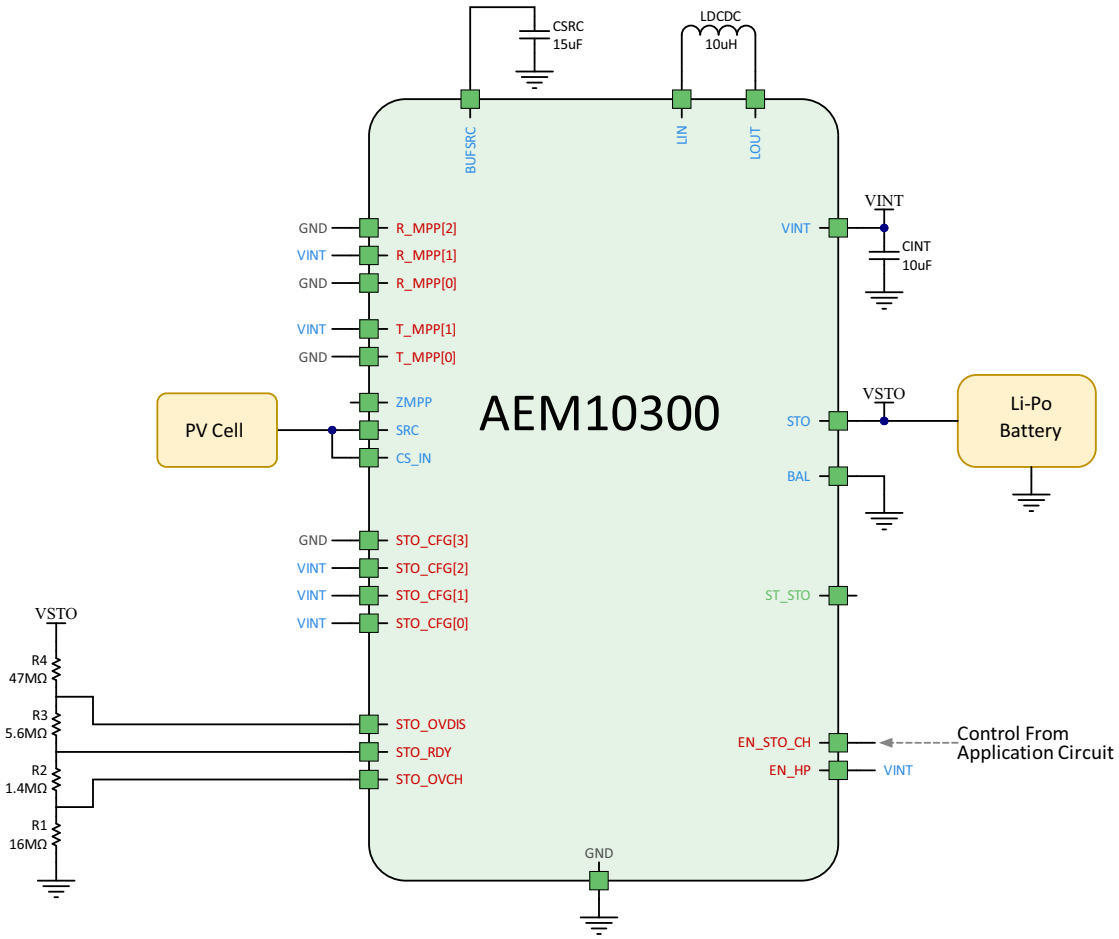


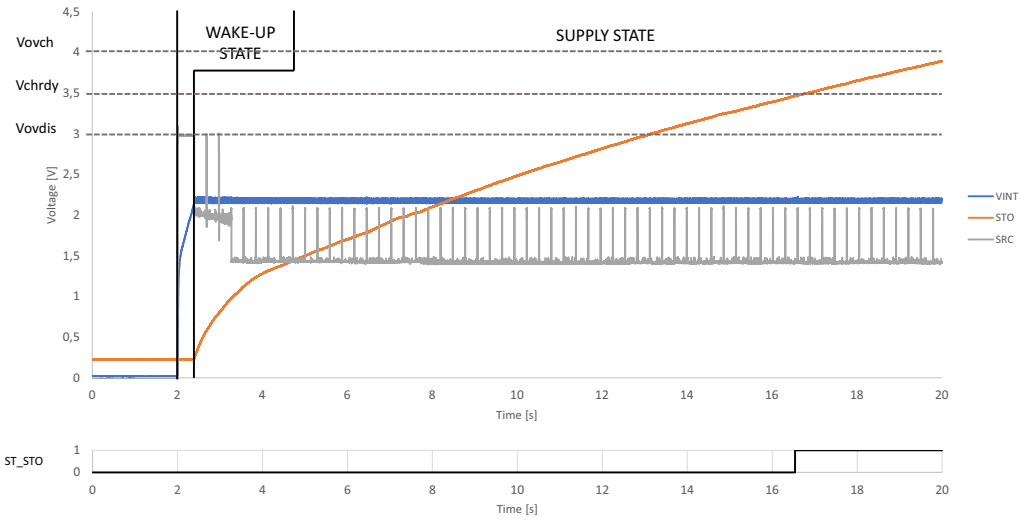
Figure 9: Typical Application Circuit 2

The circuit is an example of a system with solar energy harvesting. It uses a Li-Po rechargeable battery as energy storage, which voltages thresholds are set by the custom mode.

Please note that the custom mode is used for the sake of the example, but most applications that use a Li-Po battery as storage element could use a pre-defined mode that does not require to implement the resistive divider (R1-R2-R3-R4), and thus have a reduced bill of material compared to the circuit shown on Figure 23.

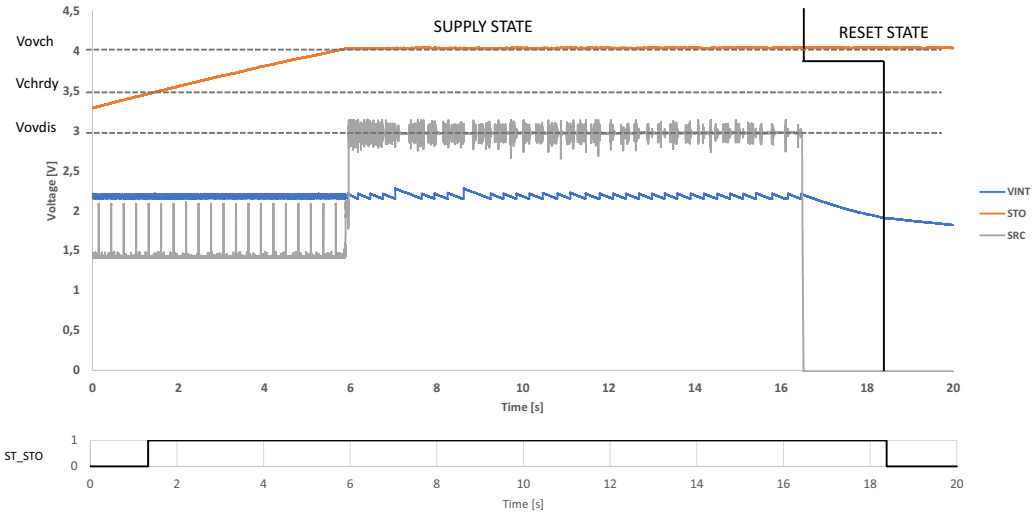
- Energy source: PV cell
- R_MPP[2:0] = 010: the MPP ratio is set to 70%
- T_MPP[1:0] = 10: the MPP sampling period is 17.87s and the MPP sampling duration is 280 ms.
- STO_CFG[3:0] = 0111: the storage element is a Li-Po rechargeable battery, used with custom mode (in this example we set V_{CHRDY} to 4.0V instead of the 3.51V on STO_CFG[3:0] = 1101 preset):
  - V_{OVCH} = 4.35V
  - V_{CHRDY} = 4.00V
  - V_{OVDIS} = 3.03V
- Custom mode resistor divider calculations (values have been rounded to the closest available value):
  - RT = 70MΩ
  - R1 = 70MΩ * (1V / 4.35V) ≈ 16MΩ
  - R2 = 70MΩ * (1V / 4.00V - 1V / 4.35V) ≈ 1.4MΩ
  - R3 = 70MΩ * (1V / 3.03V - 1V / 4.00V) ≈ 5.6MΩ
  - R4 = 70MΩ * (1 - 1V / 3.03V) ≈ 47MΩ
- BAL is not used (not a dual-cell storage element) so it is connected to GND.
- EN_HP is connected to VINT: the DCDC converter is in HIGH POWER MODE

9.3. Circuit Behaviour



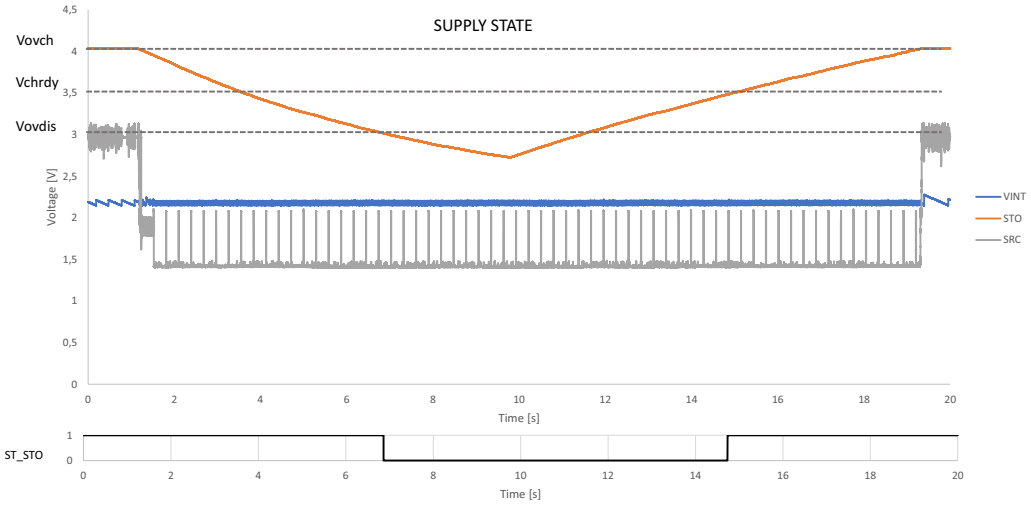
STO_CFG[3:0] = LLLL, R_MPP[2:0] = LHL, T_MPP[1:0] = LL, Storage element: capacitor (10 mF), SRC: current source (5mA) with voltage compliance (3V), EN_HP = H, EN_STO_FT = L, EN_STO_CH = H

Figure 10: Wake-up state, Start state and Supply state



STO_CFG[3:0] = LLLL, R_MPP[2:0] = LHL, T_MPP[1:0] = LL, Storage element: capacitor (10 mF), SRC: current source (5mA) with voltage compliance (3V) (stop after 16.6 s), EN_HP = H, EN_STO_FT = L, EN_STO_CH = H

Figure 11: Supply state and Reset state



STO_CFG[3:0] = LLLL, R_MPP[2:0] = LHL, T_MPP[1:0] = LL, Storage element: capacitor (10 mF), SRC: current source (5mA) with voltage compliance (3V), EN_HP = H, EN_STO_FT = L, EN_STO_CH = H, load on STO : 1K (place between 1.2 s and 9.8s)

Figure 12: Supply state

10. Performance Data

10.1. DCDC Conversion Efficiency From SRC to STO in Low Power Mode

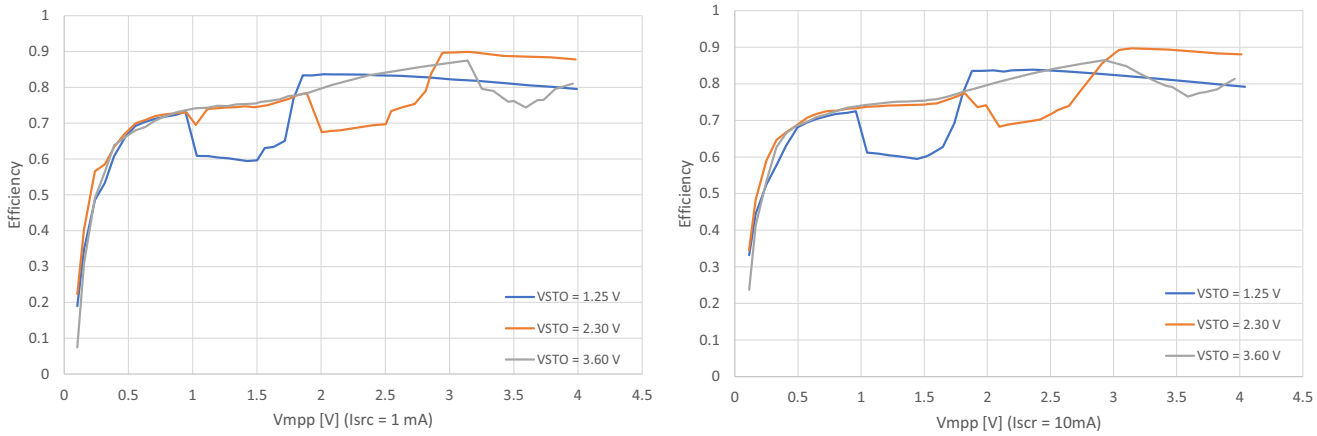


Figure 13: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode

10.2. DCDC Conversion Efficiency From SRC to STO in High Power Mode

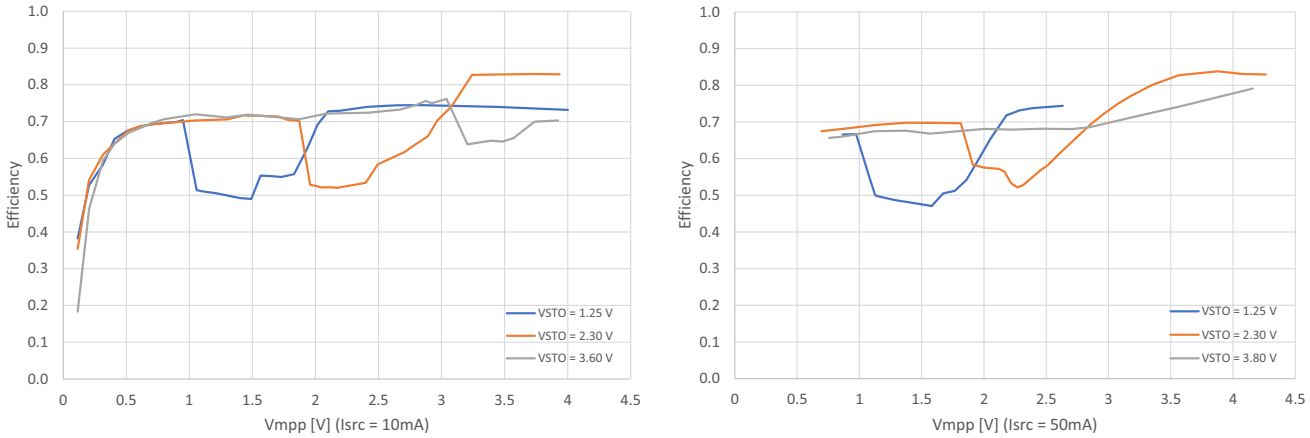


Figure 14: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode

11. Schematic

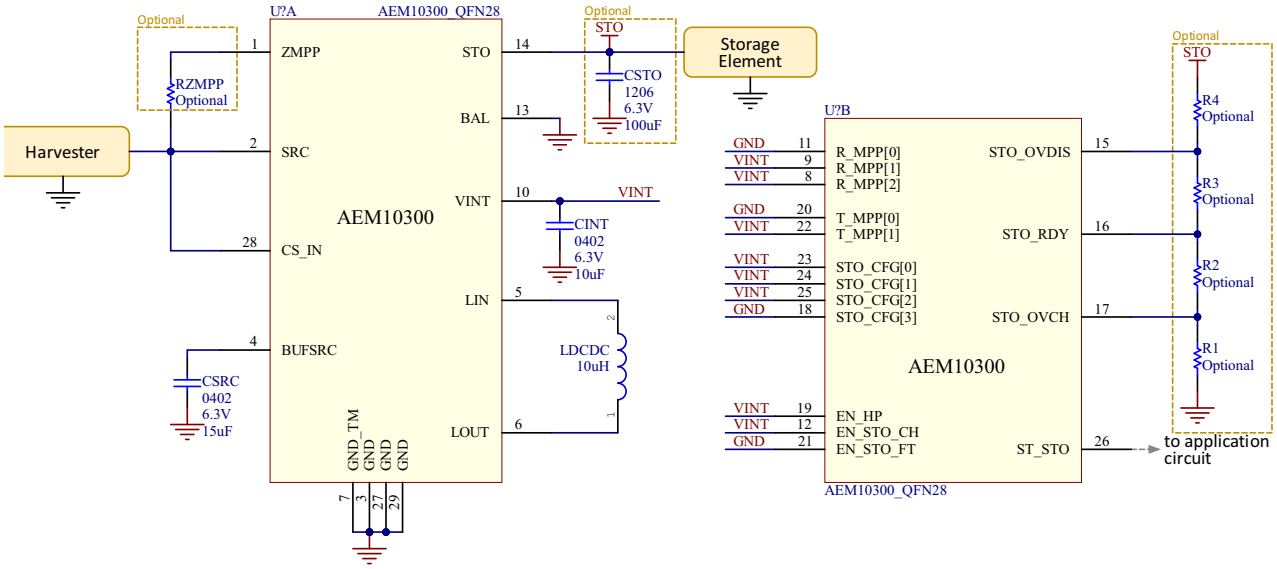


Figure 15: Schematic Example

Designator	Description	Quantity	Manufacturer	Link
U1	AEM10300 - Symbol QFN 28-pin	1	e-peas	order at sales@e-peas.com
LDCDC	Power inductor 10 µH - 1.76A	1	Murata	DFE252010F-100M
CINT	Ceramic Cap 10 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
CSRC	Ceramic Cap 15 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J156ME05
CSTO (optional)	Ceramic Cap 100 µF, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Table 12: Minimal Bill of Materials

12. Layout

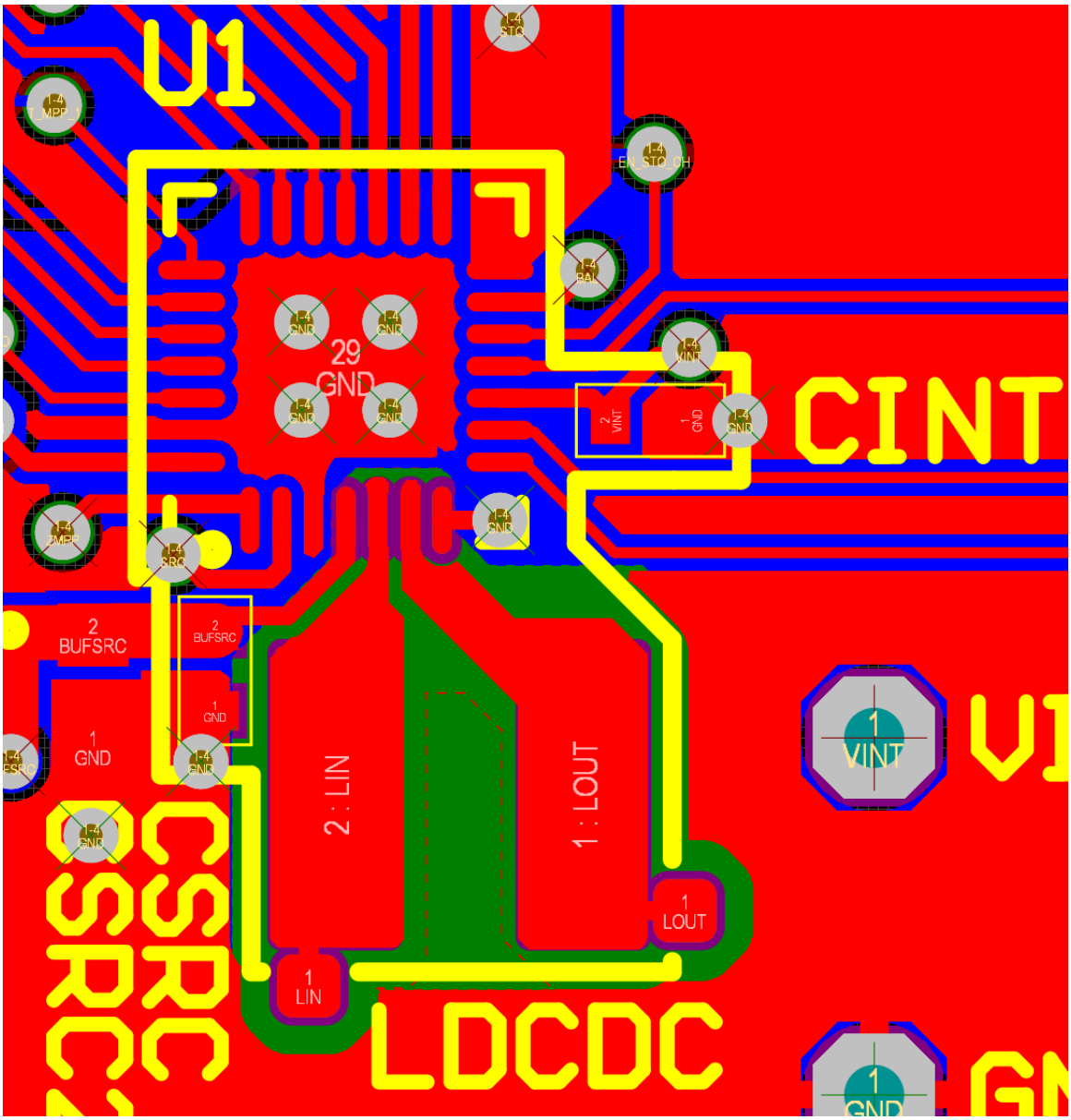


Figure 16: Layout Example for the AEM10300 and its Passive Components

NOTE: schematic, symbol and footprint for the e-peas component can be ordered by contacting e-peas support team at support@e-peas.com

13. Package Information

13.1. Plastic Quad Flatpack No-Lead (QFN 28-pin 4x4mm)

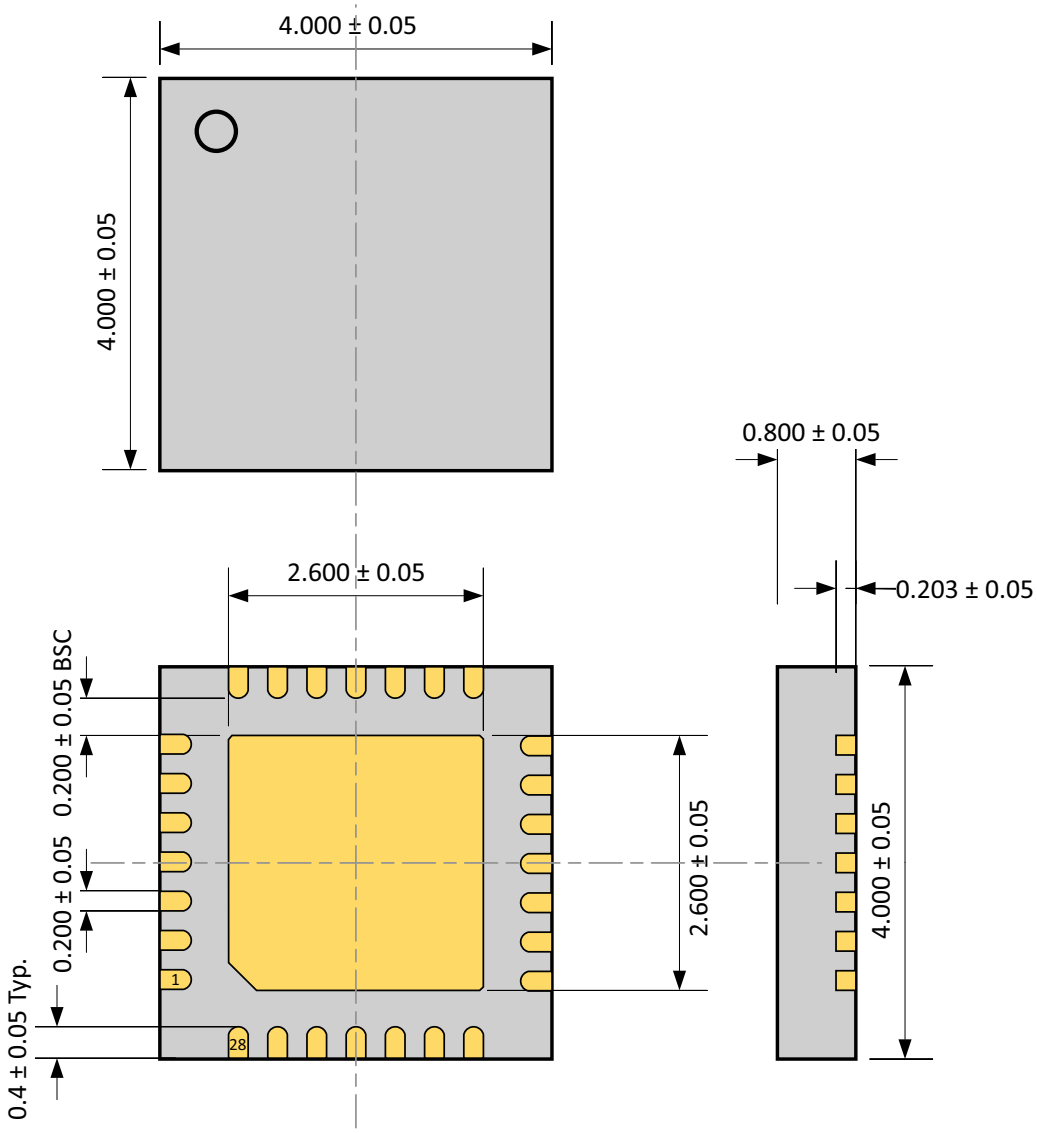


Figure 17: QFN 28-pin 4x4mm Drawing (All Dimensions in mm)

13.2. Board Layout

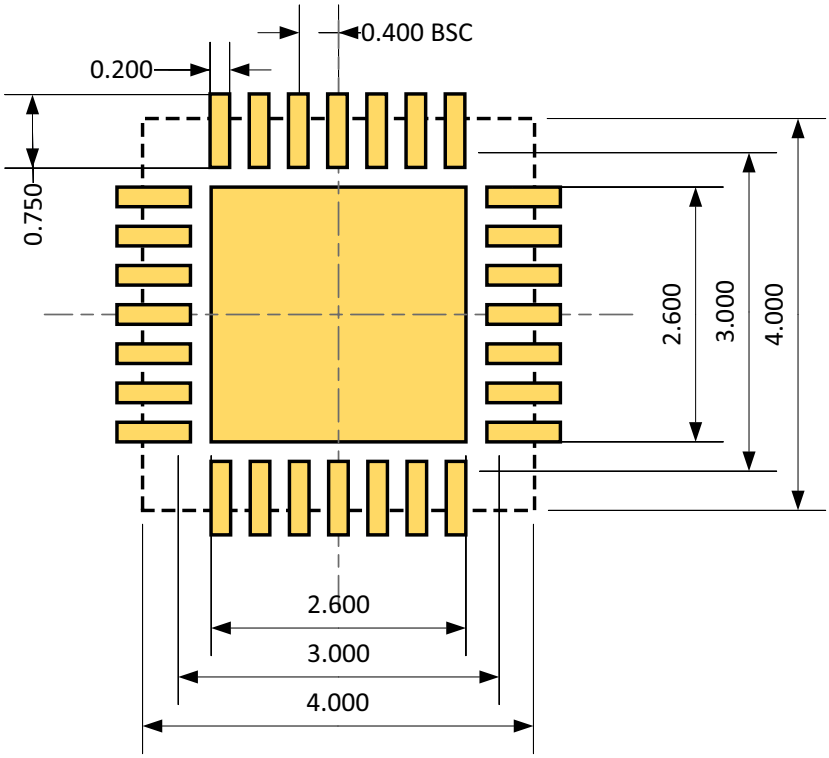


Figure 18: Recommended Board Layout (All Dimensions in mm)

14. Revision History

Revision	Date	Description
0.0	January, 2021	Creation of the document. Preliminary version.
1.0	June, 2021	First version of the document
1.1	August, 2021	Minor modifications

Table 13: Revision History