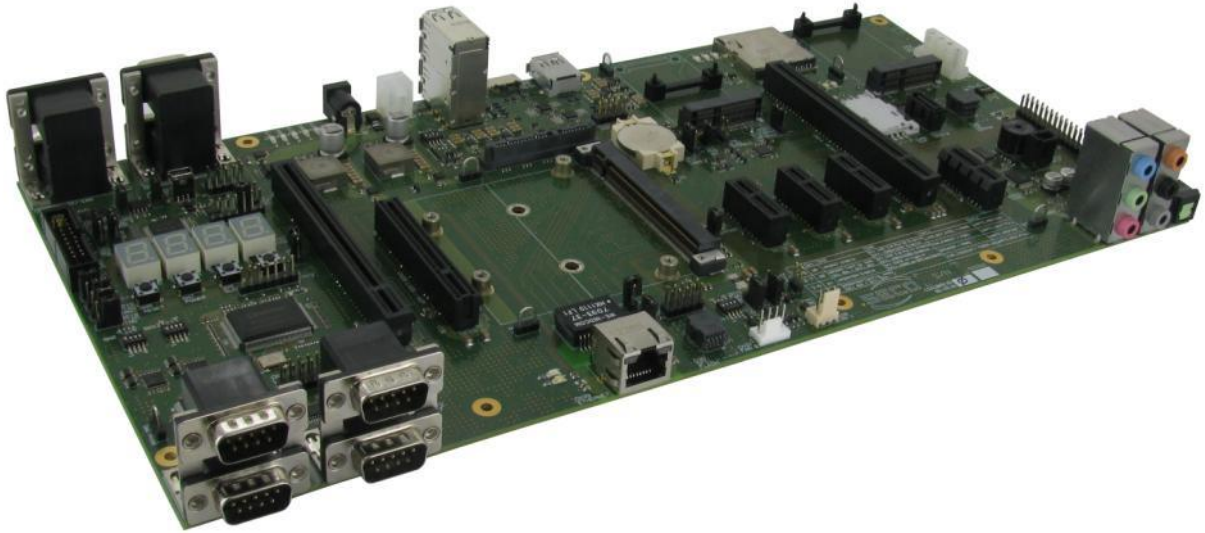
Qseven

User Manual



CQ7-A30

Cross Platform Carrier Board for Qseven®
Rel.2.0 Compliant modules

SECO

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	7th May 2015	First official release	SB
2.0	26th January 2016	Product name Change	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.r.l. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.r.l. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

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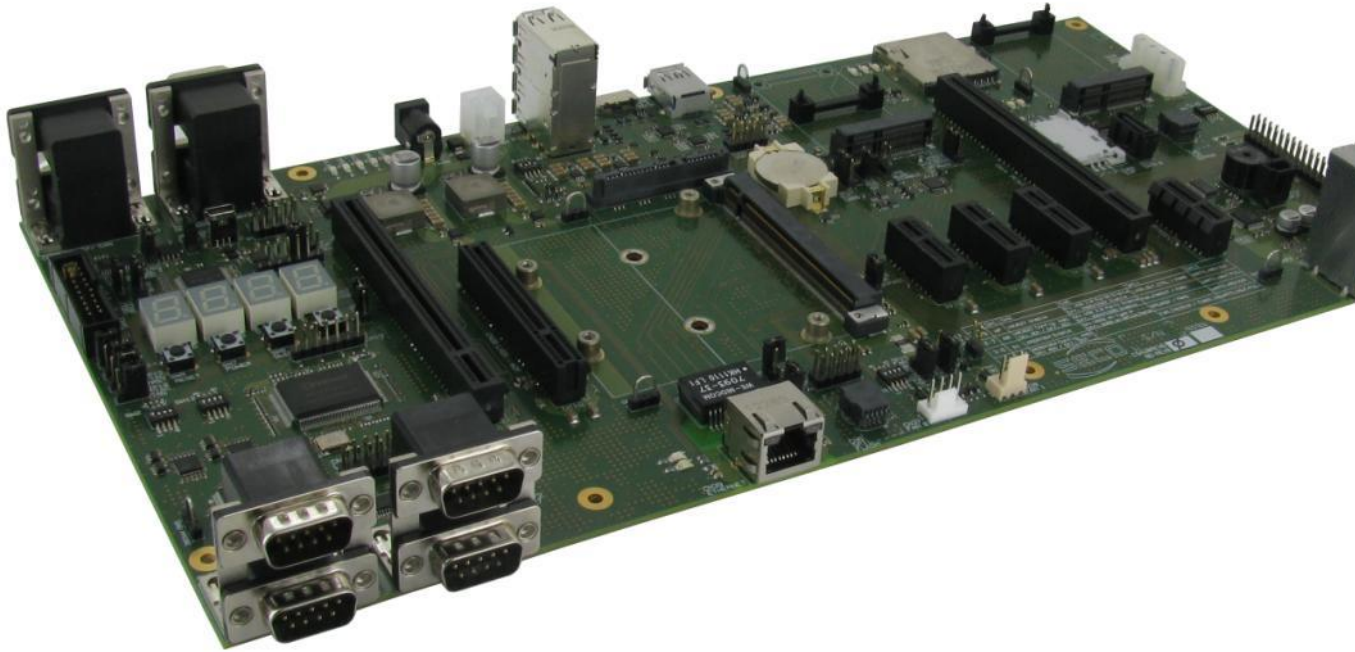
Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment and could void the warranty.

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before requesting for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be released within 1 working day (only for on-line RMA requests).

1.4 Safety

The CQ7-A30 board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The CQ7-A30 board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a CQ7-A30 board, ground yourself through an anti-static wrist strap. Placement of the board on an antistatic surface is also highly recommended.

1.6 RoHS compliance

The CQ7-A30 board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AC'97	Audio Codec'97, a standard for audio hardware codecs developed by Intel® in 1997
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
CPLD	Complex Programmable Logic Device, types of programmable logical devices
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MMC	MultiMedia Card, a type of memory card, with same interface of SD.
N.A.	Not Applicable

N.C.	Not Connected
OS	Operating System
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SIM	Subscriber Identity Module, a card which stores all data of the owner necessary to allow him accessing to mobile communication networks
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin

1.8 Reference specifications

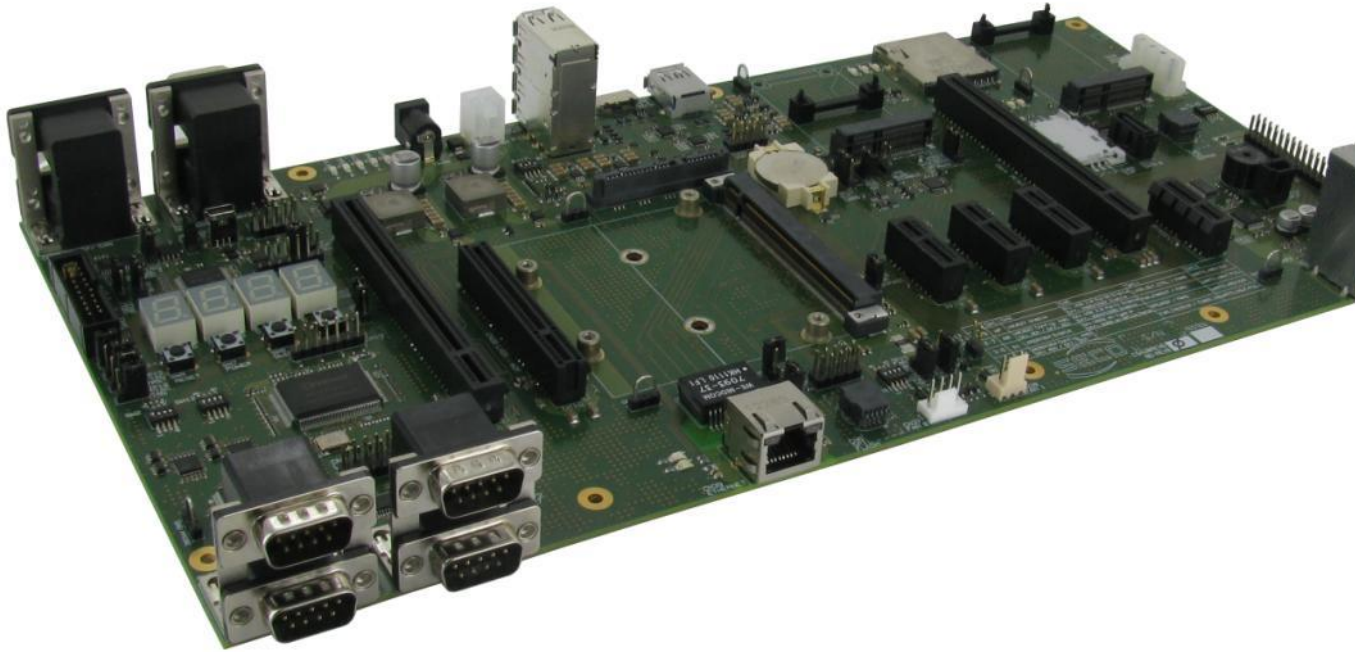
Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AC'97	http://download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
MMC	http://www.jedec.org/committees/jc-649
PCI Express	http://www.pcisig.com/specifications/pciexpress
Qseven® Design Guide	http://www.sget.org/uploads/media/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET.pdf
Qseven® Errata to Rel. 2.0	http://www.sget.org/uploads/media/Qseven-Spec_2.0_SGET_errata_sheet_E2.00-001.pdf
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs

TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

CQ7-A30 is a carrier board for Qseven® rel. 2.0 compliant modules, specifically designed to support and test the features included in the release 2.0 of the specifications, including those introduced with the Errata to rel. 2.0 published by SGET consortium.

Qseven® is a form factor designed to minimize space consumption, since it integrates in only 70x70mm of space all core components of a common PC architecture (CPU, RAM, Graphic, audio, etc.). All the functionalities are made available through a standardized card edge connector, from which all signals can be taken and carried to the appropriate external connector in the carrier board and/or to other internal component, to implement more functionalities other than those included in the standard Qseven® bus interface.

The connection to the Qseven® board is implemented through a standardized MXM connector, which is a proven high speed signal interface connector.

All the features on the CQ7-A30 board are implemented according to the Qseven® standard bus interface, thus the board is fully Qseven® Rel. 2.0 compliant and compatible with Qseven® Spec. 2.0 modules. Furthermore, the board can take advantage of all possible features that can be offered by x86 and/or ARM architectures on Qseven® modules.

The list of features that can effectively be used depends on the Qseven® module used on the Carrier Board.

CQ7-A30 board is specially designed for being an advanced development board, for skilled users who want to design their own carrier boards. Indeed, the electrical schematics of the boards included in the Development Kit will be available for developers that begin testing with this board, and want to recycle portions of it for their own-designed Carrier Boards, allowing thus a significant reduction of time for Hardware Development.

“Recycling” of the schematic is also useful for Software Development, since SECO offers also the BSP and/or drivers for the Qseven® boards used with the Development board. By using the same components in customer’s own design, a great spare in Software Development can be achieved.

The schematics of CQ7-A30 have also been used as a base for the writing of the “Qseven® Design Guide Version 2.0”. Indeed, this is the board that is indicated as the Qseven V2.0 reference Carrier Board.

Both Windows (Embedded and standard versions) and Linux are supported.

All the materials is available through web-site http://www.seco.com/, where it is possible to find any kind of information needed, and is also possible to ask for help of SECO’s Developers team to solve technical issues related to customer’s development.

2.2 Technical Specifications

Supported Modules

Qseven® Rel. 2.0 compliant modules

Mass Storage interfaces

SATA Female 7p connector with dedicated Power connector, interface shared with mSATA Slot

SATA Male 7+15p connector

SD/MMC Card Slot

SPI Flash Sock

I2C EEPROM Socket

Video Interfaces

HDMI / Display port interface on PCI-e x16 slot

LVDS / eDP interface on PCI-e x8 slot

USB

1 x USB3.0 Host port on type-A socket

1 x USB 3.0 OTG port on micro-AB socket

2 x USB2.0 Host ports on internal pin header (alternative to USB 3.0 port #0)

Up to 4 x USB2.0 Host ports on quad Type-A socket

PCI Express

PCI-e x 4 interface on dedicated PCI-e x 16 slot **shared** with 3 x PCI-e x1 slots + miniPCI-e slot (selection via jumper)

Networking

Gigabit Ethernet connector

Audio

Embedded HD Audio Codec, Realtek ALC888

2 x Triple HD Audio jacks

2 x S/P-DIF connectors (In & Out)

Audio Expansion Slot

Serial Ports

CAN Bus (both at TTL interface on internal pin header, and with CAN transceiver on DB9 connector)

3 x RS-232 only ports

2 x RS-232/RS/422/RS-485 configurable serial ports

Other Interfaces

Feature Connector, with I2C, SM Bus, Watchdog, Thermal and Power Management Signals

LPC Bus Header

SPI Pin Header

SIM Card slot

4 x 7-segment LCD displays for POST codes

PS/2 Mouse/keyboard internal pin strip

2 x tachometric FAN connectors

Power, Reset, LID and Sleep Buttons

Debug Port on mini-B USB connector

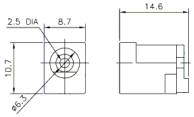
Power supply: +12V_{DC} power Jack and Mini-fit Standard ATX power connector
Coin cell battery Holder for CMOS and RTC

Operating temperature: 0°C ÷ +60°C (commercial temperature range) *

Dimensions: 345 x 170 mm (13.58" x 6.69")

! ** Temperature ranges indicated mean that all components available onboard are certified for working with a Tcase included in these temperature ranges. This means that it is customer's responsibility to ensure that all components' Tcases remain in the range above indicated.*

2.3 Electrical Specifications



CQ7-A30 board needs to be supplied using a standard ATX Power Supply (only +12V_{DC} ± 5% voltage is needed).

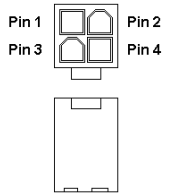
This voltage can be supplied through a standard 6.3mm (internal pin, diameter 2.5 mm) DC Power Jack, CN40. Internal pin is VIN power line.

Alternatively, it is possible to use an internal Molex Mini-Fit Jr. connector, p/n 39-28-1043, or equivalent, with the pinout indicated in the following table.

Power Connector - CN30			
Pin	**Signal**	**Pin**	**Signal**
1	GND	3	+12V_A
2	GND	4	+12V_A

The mating Connector is MOLEX p/n 39-01-3042 or equivalent, with female crimp terminal MOLEX series 5566. The use of wires with section 18 AWG or 20AWG is recommended, in order to ensure the proper amperage of the power section.

All the voltages that are necessary for board's working are derived internally from +12V_A power rail.



! Never use two different PSUs connected simultaneously to Power connectors CN30 and CN40

When choosing the power supply unit for CQ7-A30 board, please take into account all the possible consumptions of the Qseven® module and of all the external devices and/or the adapter boards connected to the system, which take their power supply directly from the carrier board.

This way it will be possible to choose a PSU capable to supply enough current for the whole system.

2.3.1 RTC Battery

For the occurrences when the system (Carrier Board + Qseven® module) is not powered with an external power supply, on board there is a horizontal battery holder, for the use of standard coin cell batteries type CR2032 with a nominal capacity of 220mAh, to supply, with a 3V voltage, the Real Time Clock and CMOS memory mounted on the Qseven® module.

JP13 position	VCC_RTC voltage
1-2	Coming from Coin Cell Battery
2-3	Tied to GND through 1kΩ resistor

It is possible to exclude the coin cell battery from supplying the VCC_RTC pin, simply by jumper JP13, , which is a standard pin header, P2.54mm, 1x3 pin, according to the table on the left.

The batteries should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.
Never allow the batteries to become short-circuited during handling.

! **CAUTION**: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Batteries supplied with CQ7-A30 board are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out

of order CQ7-A30 board, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. When replacing the batteries, the disposal too has to be made according to these requirements.

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U

+5V_SB_Q7: Qseven Module Standby voltage. This power rail is used exclusively to supply the Standby power rail of the Qseven® module plugged in slot CN1.

JP23 position	AT/ATX mode
1-2	ATX mode (switched power rails available)
2-3	AT mode (switched and always power rails correspondence)

In all the cases when switched power rails are not required (including +5V_SB_Q7, it is possible to use the jumper JP23, which is a standard pin header, P2.54mm, 1x3 pin.

2.3.3 Power LEDs

In order to show the voltage presence of specific power rails, onboard there are five LEDs.

Red LED D18: +12V_A power rail active.

Red LED D19: +5V_A power rail active.

Green LED D21: +12V_S power rail active.

Green LED D22: +5V_S power rail active.

Green LED D23: +3.3V_S power rail active.

All five LEDs are off only when the board doesn't receive any power supply input.

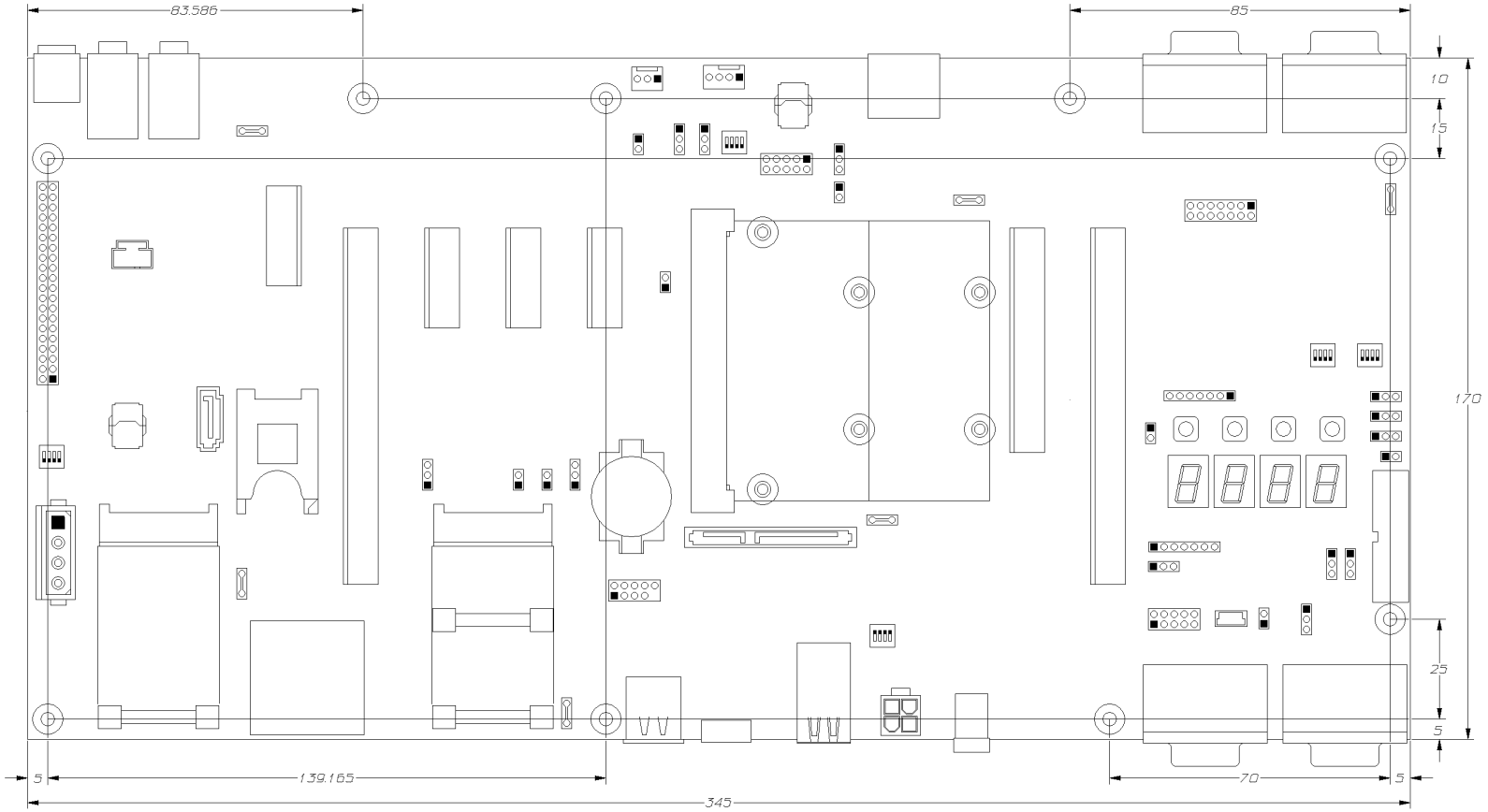
2.4 Mechanical Specifications

The board dimensions are 345 x 170 mm (13.58” x 6.69”).

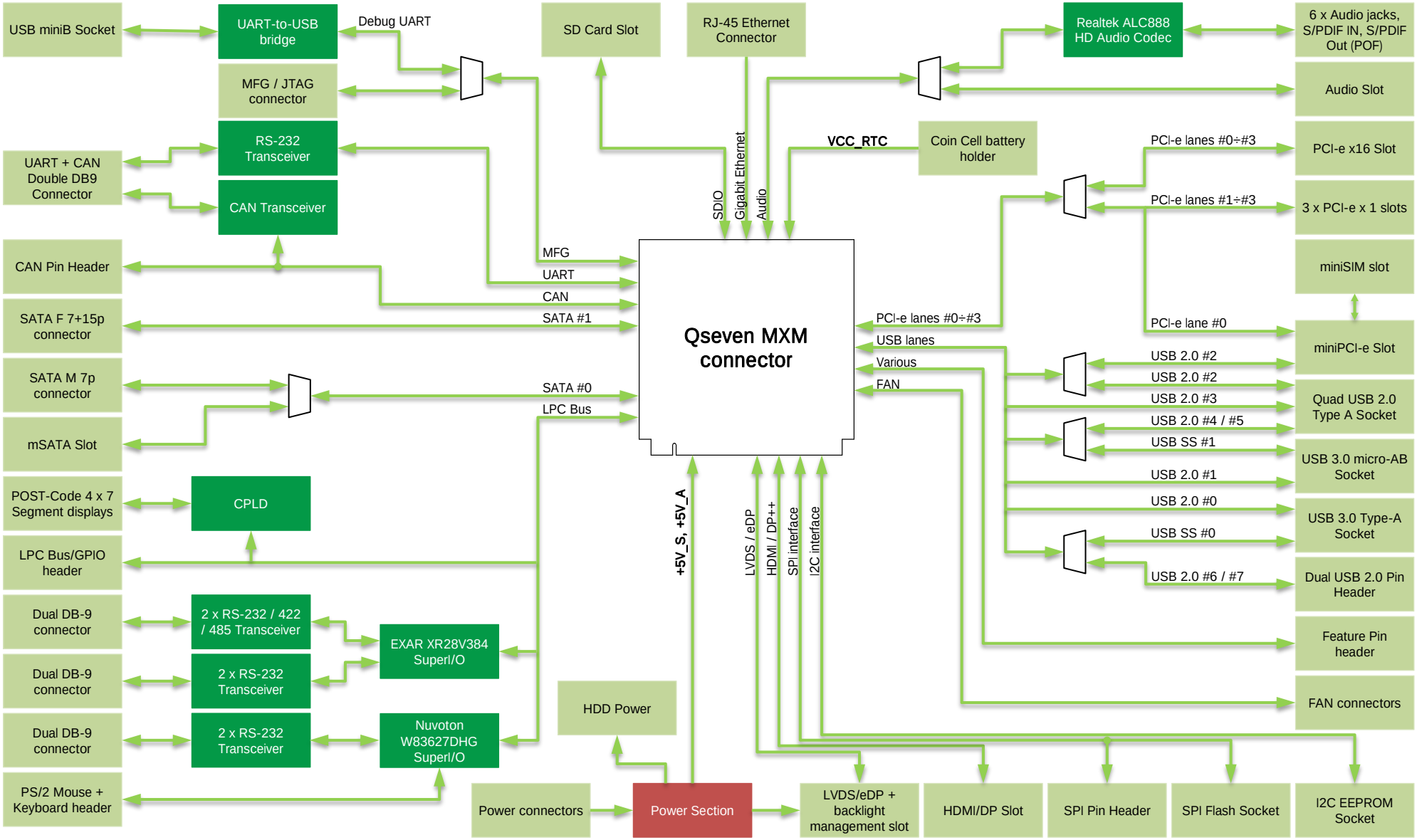
Printed circuit of the board is made of six layers, some of them are ground planes, for disturbance rejection.

In order to fix the Qseven® module to the carrier board, on CQ7-A30 are soldered four metallic spacers, height 5mm, 2.5mm diameter, that can be used for the fixing of standard size Qseven® modules.

It is possible to solder two further spacers for fixing of µQseven® modules. They are not directly soldered on the evaluation platform since the spacers needed for fixing of µQseven® modules would interfere with electronic devices soldered on standard Qseven® modules.

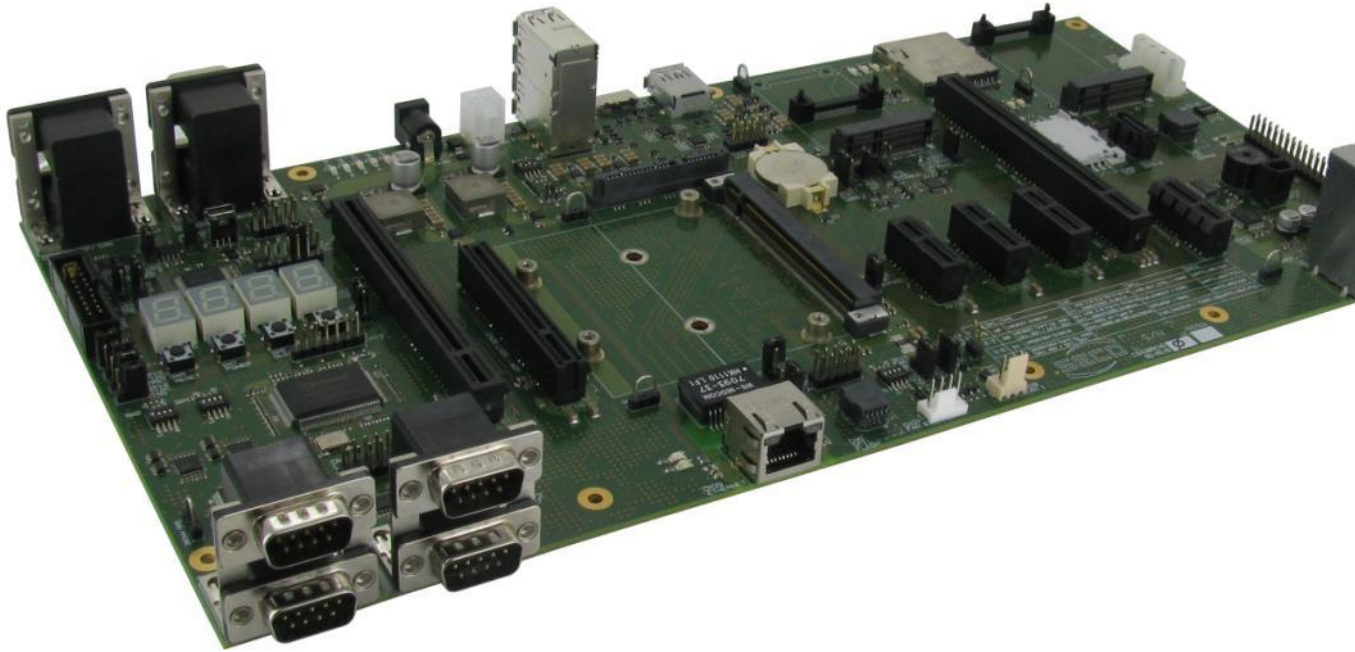


2.5 Block Diagram

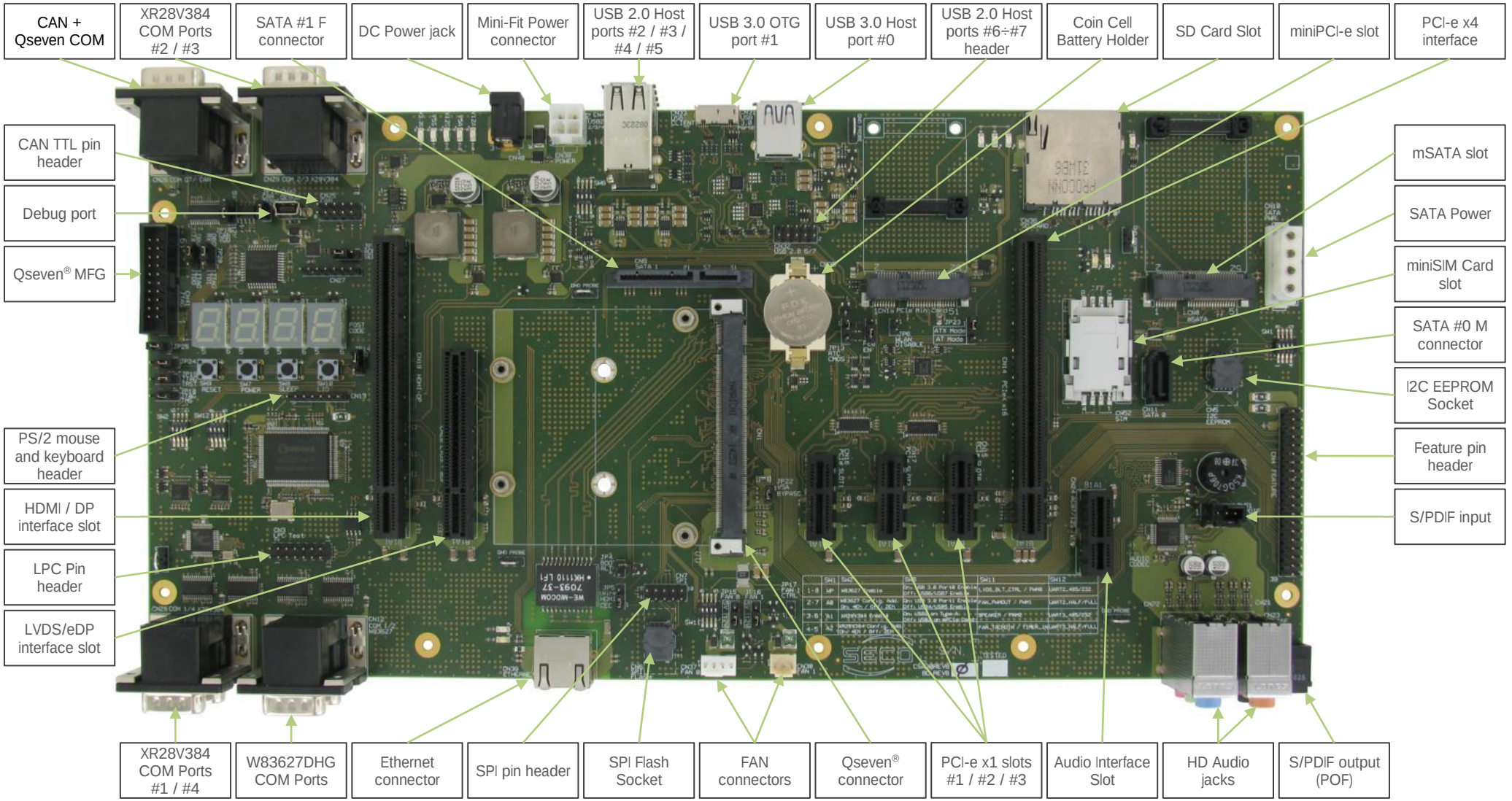


Chapter 3.
OVERVIEW

- Connectors placement
- Connectors overview
- Connectors description



3.1 Connectors placement



3.2 Connectors overview

3.2.1 Connectors list

Name	Description	Name	Description
CN1	Qseven® connector	CN23	S/PDIF Optical connector (POF)
CN3	LPC/GPIO pin header	CN24	Audio Interface Slot
CN4	Feature pin header	CN25	CAN TTL pin header
CN5	I2C EEPROM Socket	CN26	CAN + Qseven UART (RS-232) double DB9 connector
CN6	SPI Flash Socket	CN28	XR28V384 COM #1 / #4 double DB9 connector (RS-232 only)
CN7	SPI pin header	CN29	XR28V384 COM #2 / #3 double DB9 connector (RS-232 / RS-422 / RS-485 configurable)
CN8	mSATA slot	CN30	Power connector
CN9	SATA #1 F 7+15p connector	CN31	USB 3.0 Host port #0 Type-A receptacle
CN10	SATA Power connector	CN32	USB 2.0 Host ports #6 / #7 pin header
CN11	SATA #0 M 7p connector	CN33	USB 3.0 OTG port #1 micro-AB receptacle
CN12	W83627DHG Serial ports #1 / #2 double DB9 connector	CN35	Coin Cell Battery Holder
CN13	PS/2 Mouse and Keyboard header	CN36	SD Card Slot
CN14	PCI-e x16 Slot	CN37	4-poles FAN connector #0
CN15	PCI-e x1 Slot #1	CN38	3-poles FAN connector #1
CN16	PCI-e x1 Slot #2	CN39	Gigabit Ethernet connector
CN17	PCI-e x1 Slot #3	CN40	DC Power Jack
CN18	miniPCI-e Slot	CN41	MFG connector
CN19	DP++/HDMI slot	CN42	Debug port USB micro-B connector
CN20	LVDS/eDP slot	CN49	USB 2.0 Host ports #2 / #3 / #4 / #5 Quad Type-A receptacle
CN21	Triple Audio Jack 1	CN51	S/PDIF Input connector
CN22	Triple Audio Jack 2	CN52	miniSIM Card slot

3.2.2 Jumpers list

Name	Description	Name	Description
JP1	PCI-e lanes routing selection	JP16	FAN #1 voltage selection
JP4	Boot source selection	JP17	FAN #1 PWM control enable
JP5	GP_1-Wire Bus mode selector	JP18	MFG_NC3 Pull-up or pull-down
JP6	miniPCI-e Wireless operations enable	JP19	MFG_NC4 Pull-up or pull-down
JP10	CAN voltage selector	JP20	MFG_NC2 routing to MFG or Debug USB connector
JP11	120Ω CAN termination	JP21	MFG_NC1 routing to MFG or Debug USB connector
JP12	POST Codes address selector	JP23	AT/ATX mode selection
JP13	Battery/batteryless selection	JP24	SRST# source selection
JP14	LIDBTN#	JP25	MFG_NC4 connection on CN41 pin #3
JP15	FAN #0 voltage selection		

3.2.3 Dip Switch list

Name	Description	Name	Description
SW1	I2C EEPROM Address select	SW11	GP_PWM / GP_Timer selector
SW2	SuperIOs enable and address select	SW12	XR28V384 COM #2 / #3 mode selector
SW6	USB 3.0 / 2.0 ports selector		

3.3 Connectors description

3.3.1 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

NOTE: Even pins are available on top side of Qseven® module; odd pins are available on bottom side of Qseven® module.

Qseven® Connector - CN1

BOTTOM SIDE			TOP SIDE		
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
Power Ground	GND	1	2	GND	Power Ground
Gigabit Ethernet differential pair 3-	GBE_MDI3-	3	4	GBE_MDI2-	Gigabit Ethernet differential pair 2-
Gigabit Ethernet differential pair 3+	GBE_MDI3+	5	6	GBE_MDI2+	Gigabit Ethernet differential pair 2+
Ethernet 100Mb/s link indicator	GBE_LINK100#	7	8	GBE_LINK1000#	Ethernet 1000Mb/s link indicator
Gigabit Ethernet differential pair 1-	GBE_MDI1-	9	10	GBE_MDI0-	Gigabit Ethernet differential pair 0-
Gigabit Ethernet differential pair 1+	GBE_MDI1+	11	12	GBE_MDI0+	Gigabit Ethernet differential pair 0+
Ethernet link indicator	GBE_LINK#	13	14	GBE_ACT#	Ethernet Activity indicator
Ethernet Reference Voltage	GBE_CTREF	15	16	SUS_S5#	Soft Off (S5) output Signal
Wake Input	WAKE#	17	18	SUS_S3#	Suspend to RAM (S3) output signal
Suspend Status Output	SUS_STAT#	19	20	PWRBTN#	Power Button Input
Sleep Button Input	SLP_BTN#	21	22	LID_BTN#	LID Button Input
Power Ground	GND	23	24	GND	Power Ground
Power Ground	GND	25	26	PWGIN	Qseven® module Power Good Input
Battery Low Input	BATLOW#	27	28	RSTBTN#	Reset Button Input
Serial ATA Channel 0 Transmit +	SATA0_TX+	29	30	SATA1_TX+	Serial ATA Channel 1 Transmit +
Serial ATA Channel 0 Transmit -	SATA0_TX-	31	32	SATA1_TX-	Serial ATA Channel 1 Transmit -
Serial ATA Activity LED output	SATA_ACT#	33	34	GND	Power Ground
Serial ATA Channel 0 Receive +	SATA0_RX+	35	36	SATA1_RX+	Serial ATA Channel 1 Receive +
Serial ATA Channel 0 Receive -	SATA0_RX-	37	38	SATA1_RX-	Serial ATA Channel 1 Receive -

Power Ground	GND	39	40	GND	Power Ground
Module alternate Boot Input	BIOS_DISABLE#/BOOT_ALT#	41	42	SDIO_CLK	SDIO Clock
SDIO Card Detect Input	SDIO_CD#	43	44	SDIO_LED	SDIO Activity LED output
SDIO Command/Response	SDIO_CMD	45	46	SDIO_WP	SDIO Write Protect, tied to GND (disabled)
SDIO Power Enable output	SDIO_PWR#	47	48	SDIO_DAT1	SDIO Data Line 1
SDIO Data Line 0	SDIO_DAT0	49	50	SDIO_DAT3	SDIO Data Line 3
SDIO Data Line 2	SDIO_DAT2	51	52	SDIO_DAT5	SDIO Data Line 5
SDIO Data Line 4	SDIO_DAT4	53	54	SDIO_DAT7	SDIO Data Line 7
SDIO Data Line 6	SDIO_DAT6	55	56	USB_DRIVE_VBUS	USB Power Enable for USB Port #1
Power Ground	GND	57	58	GND	Power Ground
Audio Synchronization output signal	HDA_SYNC/I2S_WS	59	60	SMB_CLK	System Management Bus Clock
Audio Codec Reset, output	HDA_RST#/I2S_RST#	61	62	SMB_DAT	System Management Bus Data
Audio Bit Clock output	HDA_BCLK/I2S_CLK	63	64	SMB_ALERT#	System Management Bus Alert
Audio Serial Data Input	HDA_SDI/I2S_SDI	65	66	GP0_I2C_CLK	I^2C Bus Clock Line
Audio Serial Data Output	HDA_SDO/I2S_SDO	67	68	GP0_I2C_DAT	I^2C Bus Data Line
Thermal Alarm Input	THRM#	69	70	WDTRIG#	Watchdog Trigger Input
Thermal Trip Output	THRMTRIP#	71	72	WDOUT	Watchdog event indicator Output
Power Ground	GND	73	74	GND	Power Ground
USB 2.0 Data Port #7 - / SuperSpeed Port #0 transmit -	USB_P7-/USB_SSTX0-	75	76	USB_P6-/USB_SSRX0-	USB 2.0 Data Port #6 - / SuperSpeed Port #0 receive -
USB 2.0 Data Port #7 + / SuperSpeed Port #0 transmit +	USB_P7+/USB_SSTX0+	77	78	USB_P6+/USB_SSRX0+	USB 2.0 Data Port #6 + / SuperSpeed Port #0 receive +
USB ports 6/7 overcurrent detect	USB_6_7_OC#	79	80	USB_4_5_OC#	USB ports 4/5 overcurrent detect
USB 2.0 Data Port #5 - / SuperSpeed Port #1 transmit -	USB_P5-/USB_SSTX1-	81	82	USB_P4-/USB_SSRX1-	USB 2.0 Data Port #4 - / SuperSpeed Port #1 receive -
USB 2.0 Data Port #5 + / SuperSpeed Port #1 transmit +	USB_P5+/USB_SSTX1+	83	84	USB_P4+/USB_SSRX1+	USB 2.0 Data Port #4 + / SuperSpeed Port #1 receive +
USB ports 2/3 overcurrent detect	USB_2_3_OC#	85	86	USB_0_1_OC#	USB ports 0/1 overcurrent detect
USB Data Port #3 -	USB_P3-	87	88	USB_P2-	USB Data Port #2 -
USB Data Port #3 +	USB_P3+	89	90	USB_P2+	USB Data Port #2 +
USB VBus Input	USB_VBUS	91	92	USB_ID	USB Port 1 mode configuration output

USB Data Port #1 -	USB_P1-	93	94	USB_P0-	USB Data Port #0 -
USB Data Port #1 +	USB_P1+	95	96	USB_P0+	USB Data Port #0 +
Power Ground	GND	97	98	GND	Power Ground
LVDS or eDP primary channel pair 0 +	LVDS_A0+ / eDP0_TX0+	99	100	LVDS_B0+ / eDP1_TX0+	LVDS or eDP secondary channel pair 0 +
LVDS or eDP primary channel pair 0 -	LVDS_A0- / eDP0_TX0-	101	102	LVDS_B0- / eDP1_TX0-	LVDS or eDP secondary channel pair 0 -
LVDS or eDP primary channel pair 1 +	LVDS_A1+ / eDP0_TX1+	103	104	LVDS_B1+ / eDP1_TX1+	LVDS or eDP secondary channel pair 1 +
LVDS or eDP primary channel pair 1 -	LVDS_A1- / eDP0_TX1-	105	106	LVDS_B1- / eDP1_TX1-	LVDS or eDP secondary channel pair 1 -
LVDS or eDP primary channel pair 2 +	LVDS_A2+ / eDP0_TX2+	107	108	LVDS_B2+ / eDP1_TX2+	LVDS or eDP secondary channel pair 2 +
LVDS or eDP primary channel pair 2 -	LVDS_A2- / eDP0_TX2-	109	110	LVDS_B2- / eDP1_TX2-	LVDS or eDP secondary channel pair 2 -
LCD Panel Power Enable	LVDS_PPEN	111	112	LVDS_BLEN	LCD Panel Backlight Enable
LVDS or eDP primary channel pair 3 +	LVDS_A3+ / eDP0_TX3+	113	114	LVDS_B3+ / eDP1_TX3+	LVDS or eDP secondary channel pair 3 +
LVDS or eDP primary channel pair 3 -	LVDS_A3- / eDP0_TX3-	115	116	LVDS_B3- / eDP1_TX3-	LVDS or eDP secondary channel pair 3 -
Power Ground	GND	117	118	GND	Power Ground
LVDS primary channel Clock + or eDP primary auxiliary channel +	LVDS_A_CLK+ / eDP0_AUX+	119	120	LVDS_B_CLK+ / eDP1_AUX+	LVDS secondary channel Clock + or eDP secondary auxiliary channel +
LVDS primary channel Clock + or eDP primary auxiliary channel -	LVDS_A_CLK- / eDP0_AUX-	121	122	LVDS_B_CLK- / eDP1_AUX-	LVDS secondary channel Clock - or eDP secondary auxiliary channel -
LCD Panel brightness control / General Purpose PWM Out 0	LVDS_BLT_CTRL / GP_PWM_OUT0	123	124	GP_1-Wire_Bus	General Purpose 1-Wire bus interface
LVDS DisplayID Data Line	LVDS_DID_DAT	125	126	eDP0_HPD#	Primary eDP Hotplug detection
LVDS DisplayID Clock Line	LVDS_DID_CLK	127	128	eDP1_HPD#	Secondary eDP Hotplug detection
CAN Port Transmit line	CAN_TX	129	130	CAN_RX	CAN Port Receive line
TMDS Clock + or DP Data Line 3+	TMDS_CLK+ / DP_LANE3+	131	132	RSVD_132	Reserved pin (Differential pair)
TMDS Clock - or DP Data Line 3-	TMDS_CLK- / DP_LANE3-	133	134	RSVD_134	Reserved pin (Differential pair)
Power Ground	GND	135	136	GND	Power Ground
TMDS Data Line 1+ or DP Data Line 1+	TMDS_LANE1+ / DP_LANE1+	137	138	DP_AUX+	Display Port auxiliary channel +
TMDS Data Line 1- or DP Data Line 1-	TMDS_LANE1- / DP_LANE1-	139	140	DP_AUX-	Display Port auxiliary channel -
Power Ground	GND	141	142	GND	Power Ground
TMDS Data Line 0+ or DP Data Line 2+	TMDS_LANE0+ / DP_LANE2+	143	144	RSVD_144	Reserved pin (Differential pair)
TMDS Data Line 0- or DP Data Line 2-	TMDS_LANE0- / DP_LANE2-	145	146	RSVD_146	Reserved pin (Differential pair)
Power Ground	GND	147	148	GND	Power Ground

TMDS Data Line 2+ or DP Data Line 0+	TMDS_LANE2+ / DP_LANE0+	149	150	HDMI_CTRL_DAT	HDMI I^2C Control Data Line
TMDS Data Line 2- or DP Data Line 0-	TMDS_LANE2- / DP_LANE0-	151	152	HDMI_CTRL_CLK	HDMI I^2C Control Clock Line
Display Port / HDMI Hot Plug Detect Input	DP_HDMI_HPD#	153	154	DP_HPD#	Display Port Hot Plug Detect Input
PCI-E Reference Clock +	PCIE_CLK_REF+	155	156	PCIE_WAKE#	Wake signal from ext. devices
PCI-E Reference Clock -	PCIE_CLK_REF-	157	158	PCIE_RST#	Reset signal to external devices
Power Ground	GND	159	160	GND	Power Ground
PCI-E Channel 3 Transmit +	PCIE3_TX+	161	162	PCIE3_RX+	PCI-E Channel 3 Receive +
PCI-E Channel 3 Transmit -	PCIE3_TX-	163	164	PCIE3_RX-	PCI-E Channel 3 Receive -
Power Ground	GND	165	166	GND	Power Ground
PCI-E Channel 2 Transmit +	PCIE2_TX+	167	168	PCIE2_RX+	PCI-E Channel 2 Receive +
PCI-E Channel 2 Transmit -	PCIE2_TX-	169	170	PCIE2_RX-	PCI-E Channel 2 Receive -
TTL Serial Port Transmit	UART0_TX	171	172	UART0_RTS#	TTL Serial Port Request To Send output
PCI-E Channel 1 Transmit +	PCIE1_TX+	173	174	PCIE1_RX+	PCI-E Channel 1 Receive +
PCI-E Channel 0 Transmit -	PCIE1_TX-	175	176	PCIE1_RX-	PCI-E Channel 1 Receive -
TTL Serial Port Receive signal	UART0_RX	177	178	UART0_CTS#	TTL Serial Port Clear To Send input
PCI-E Channel 0 Transmit +	PCIE0_TX+	179	180	PCIE0_RX+	PCI-E Channel 0 Receive +
PCI-E Channel 0 Transmit -	PCIE0_TX-	181	182	PCIE0_RX-	PCI-E Channel 0 Receive -
Power Ground	GND	183	184	GND	Power Ground
LPC Bus Address/Data 0 / General Purpose I/O #0	LPC_AD0/GPIO0	185	186	LPC_AD1/GPIO1	LPC Bus Address/Data 1 / General Purpose I/O #1
LPC Bus Address/Data 2 / General Purpose I/O #2	LPC_AD2/GPIO2	187	188	LPC_AD3/GPIO3	LPC Bus Address/Data 3 / General Purpose I/O #3
LPC Bus Clock / General Purpose I/O #4	LPC_CLK/GPIO4	189	190	LPC_FRAME#/GPIO5	LPC Bus Frame signal / General Purpose I/O #5
LPC Serialised Interrupt / General Purpose I/O #6	SERIRQ/GPIO6	191	192	LPC_LDRQ#/GPIO7	LPC DMA Request / General Purpose I/O #7
Battery Power Line for RTC	VCC_RTC (+3.3V_A)	193	194	SPKR / GP_PWM_OUT2	Speaker output / general purpose PWM Output 2
FAN Tachometric Input / General Purpose Timer Input	FAN_TACHOIN / GP_TIMER_IN	195	196	FAN_PWMOUT /GP_PWM_OUT1	Fan speed control / General Purpose PWM output #1
Power Ground	GND	197	198	GND	Power Ground

SPI Master Output / Slave Input	SPI_MOSI	199	200	SPI_CS0#	SPI Chip Select 0
SPI Master Input / Slave Output	SPI_MISO	201	202	SPI_CS1#	SPI Chip Select 1
SPI Clock	SPI_CLK	203	204	MFG_NC4	Manufacturer Reserved Pin
Standby Power Supply Line	+5V_SB_Q7	205	206	+5V_SB_Q7	Standby Power Supply Line
Manufacturer Reserved Pin #0	MFG_NC0	207	208	MFG_NC2	Manufacturer Reserved Pin
Manufacturer Reserved Pin #1	MFG_NC1	209	210	MFG_NC3	Manufacturer Reserved Pin
Switched Power Supply Line	+5V_S	211	212	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	213	214	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	215	216	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	217	218	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	219	220	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	221	222	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	223	224	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	225	226	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	227	228	+5V_S	Switched Power Supply Line
Switched Power Supply Line	+5V_S	229	230	+5V_S	Switched Power Supply Line

3.3.2 Boot selector jumper

Connected to pin #41 of the card edge connector, there is a two-way P 2.54mm jumper, JP4, which allows to select different booting option (which depend on the Qseven® module installed. Please refer to the Qseven® module's User Manual for more details about the effects of this signal).

JP4 position	BIOS_DISABLE#/BOOT_ALT# signal
Not inserted	Floating. Pulled-up on the Qseven® module if needed.
Inserted	Tied to GND

3.3.3 GP_1-Wire Bus mode selector

JP5 position	GP_1-Wire_Bus signal used as
1-2	1-Wire Bus
2-3	HDMI_CEC

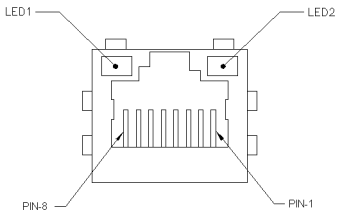
Connected to pin #124 of the card edge connector, there is a three-way P 2.54mm jumper, JP5, which allows to select if this multiplexed pin has to be used for 1-Wire bus (carried to SPI pin header CN7) or for HDMI CEC functionality (routed to the HDMI/DP interface slot CN19).

3.3.4 Ethernet connector

Gigabit Ethernet Connector- CN39			
Pin	Signal	Pin	Signal
1	GBE0_MDI0+	5	GBE0_MDI2-
2	GBE0_MDI0-	6	GBE0_MDI1-
3	GBE0_MDI1+	7	GBE0_MDI3+
4	GBE0_MDI2+	8	GBE0_MDI3-

It is possible to connect the carrier board to a network by using the Gigabit/FastEthernet interface offered by the Qseven® module used.

For this purpose, onboard there is a Gigabit Ethernet connector, CN39, type Tyco Electronics p/n 2-406549-8 or equivalent,



CN39 provide direct access to the Ethernet signals directly managed by the Qseven® modules-

On the connectors there are also two bicolour Green/Yellow LEDs.

LED1 (Left LED) is driven by Qseven® connector's signal GBE_LINK#, and shows Link connection: when it is lit, detects the availability of the connection, when the LED is Off then no connection is available.

LED2 (Right LED) is driven by Qseven® connector's signal GBE_ACT#, and shows ACTIVITY presence.

Other two LEDs on the carrier board are located near connector CN39. D33 is a green LED, driven by Qseven® connector's signal GBE_LINK100#, and shows the availability of a 10/100Mbps connection.

D34, driven by Qseven® connector's signal GBE_LINK1000#, shows the availability of a 1Gbps connection.

The interface available on connector CN39 is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. It will configure automatically to work with the existing network.

Please be aware that it will work in Gigabit mode only in case that they are connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

GBEx_MDI0+/GBEx_MDI0-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBEx_MDI1+/GBEx_MDI1-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

GBEx_MDI2+/GBEx_MDI2-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBEx_MDI3+/GBEx_MDI3-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

3.3.5 USB connectors

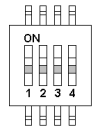
CQ7-A30 carrier board offers the possibility of connecting multiple USB devices, exploiting the USB lanes that can come out from Qseven® module.

Common mode chokes are placed on all USB differential pairs for EMI compliance. For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Since Qseven® standard offers the possibility of having up to two USB 3.0 ports, or up to eight USB 2.0 ports, onboard it is possible to select how the pins dedicated to USB ports #4 / #5 / #6 / #7 are used (if for Superspeed connection, on connectors CN31 and/or CN33, or for USB 2.0 on connectors CN49 and/or CN32).

SW6 Switch	ON Position	OFF Position
1	USB 3.0 Port #0 enabled	USB 2.0 Ports #6 / #7 Enabled
2	USB 3.0 Port #1 enabled	USB 2.0 Ports #4 / #5 Enabled
3	USB 2.0 port #2 on connector CN49	USB 2.0 port #2 on miniPCI-e slot
4	N.C.	N.C.

The selection is made using dedicated Dip switch SW6, with the meaning shown in the table on the left:

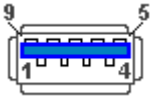


Please be aware that switches #1 and #2 must be set accordingly to the functionalities supported by the Qseven® module used (i.e., if it offers USB 3.0 or USB 2.0 interface)

USB 3.0 port #0 is available on a single USB 3.0 type-A receptacle, CN31.

USB 3.0 Host Port #0 type A receptacle - CN31

Pin	Signal	Pin	Signal
1	$+5V_{USB0}$	5	USB_SSRX0-
2	USB_P0-	6	USB_SSRX0+
3	USB_P0+	7	GND
4	GND	8	USB_SSTX0-
		9	USB_SSTX0+



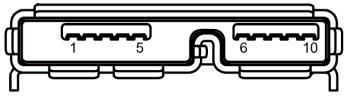
Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

The USB 2.0 Host port #0 is always available on the connector CN31 only. In case the Qseven® module used doesn't offer USB 3.0 ports, it will be always possible to use USB 2.0 port #0, simply by plugging an USB 2.0 cable.

! Please be aware that USB 3.0 connectivity can be obtained only in case that it is supported by the Qseven® module plugged into the MXM connector.
Avoid using USB 3.0 cables if the Qseven® module used doesn't offer such an interface.
Please also remember that USB SuperSpeed interface is available on CN31 only when SW6 switch #1 is set on ON position.

USB 3.0 port #1, which could offer OTG functionalities (it depends on the Qseven® module used), is available on a single USB 3.0 type micro-AB receptacle, CN33.



USB 3.0 OTG Port #1 micro-AB receptacle - CN33

Pin	Signal	Pin	Signal
1	USB_VBUS	6	USB_SSTX1-
2	USB_P1-	7	USB_SSTX1+
3	USB_P1+	8	GND
4	USB_ID	9	USB_SSRX1-
5	GND	10	USB_SSRX1+

This connector is a standard micro-AB USB 3.0 receptacle; it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using standard micro-A or micro-B USB 3.0 or USB 2.0 plugs..

A micro-A USB cable has to be used when the system has to work in Host mode. In this case, USB_VBUS is a power output of CQ7-A30 Carrier Board for the connected device.

When a micro-B USB cable is used, its USB_ID pin is floating; this way, the board acknowledges that it must configure itself to work as a Client. In this case, USB_VBUS is an input of the carrier board from the external Host.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

The USB 2.0 Host port #1 is always available on the connector CN33 only. In case the Qseven® module used doesn't offer USB 3.0 port #1, it will be always possible to use USB 2.0 port #1, simply by plugging an USB 2.0 micro-A (Host mode) or micro-B (Client mode) cable.

! Please be aware that USB 3.0 connectivity can be obtained only in case that it is supported by the Qseven® module plugged into the MXM connector.
Avoid using USB 3.0 cables if the Qseven® module used doesn't offer such an interface.
Please also remember that USB SuperSpeed interface is available on CN33 only when SW6 switch #2 is set on ON position.

Please be aware that the USB OTG port has been designed according to, published by SGET consortium, that foresee the use of signal USB_DRIVE_VBUS, present on formerly reserved pin #56.

Correct USB OTG functionalities, therefore, are ensured only for modules developed according to Qseven® Specifications rel. 2.0 Errata Sheet.

Signal description of this port:

USB_P1+/USB_P1-: USB OTG Port #1 differential pair.

USB_SSTX1-/USB_SSTX1+: USB Superspeed port#1 transmitting differential pair, switched to the micro-AB connector CN33 using the dedicated switch SW6.

USB_SSRX1-/USB_SSRX1+: USB Superspeed port#1 receiving differential pair, switched to the micro-AB connector CN33 using the dedicated switch SW6.

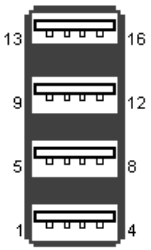
USB_VBUS: USB voltage rail. It is an input for USB port working in Client mode, an output for Host mode.

USB_ID: Client/Host identification signal. This signal is high when the USB port works in client mode, is low when works in Host mode.

USB 2.0 Host ports #2 / #3 / #4 / #5 Quad Type-A receptacle - CN49							
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	$+5V_{USB2}$	5	$+5V_{USB3}$	9	$+5V_{USB4}$	13	$+5V_{USB5}$
2	USB_P2-	6	USB_P3-	10	USB_P4-	14	USB_P5-
3	USB_P2+	7	USB_P3+	11	USB_P4+	15	USB_P5+
4	GND	8	GND	12	GND	16	GND

USB port #2 will be available on CN49 only when SW6 switch #3 is set to ON position.

Depending on the settings of Dip Switch SW6, it is possible to have up to four USB 2.0 ports, coming out from Qseven® module, are carried out on a standard quad Type-A receptacle.



Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 devices using Standard-A USB 2.0 cables.

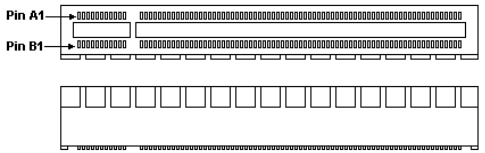
USB ports #4 and #5 will be available on CN49 only when SW6 switch #2 is set to OFF position.

USB 2.0 Host ports #6 / #7 pin header - CN32			
Pin	Signal	Pin	Signal
1	$+5V_{USB6}$	2	$+5V_{USB7}$
3	USB_P6-	4	USB_P7-
5	USB_P6+	6	USB_P7+
7	GND	8	GND
		10	N.C.

When SW6 switch #1 is set to OFF position, then USB 2.0 ports #6 and #7, coming out from the Qseven® module, will be available on an internal 9-pin standard male pin header (CN32), p 2.54 mm, 4+ 5 pin, h= 6mm, with the pinout shown in the table on the left.

For the connection of standard devices to this pin header, it is needed an adapter cable, which is included in the “Cross Platform Development Kit 2.0”.

3.3.6 DP++/HDMI Slot



The Qseven® specifications rel. 2.0 consider the possibility of having two different video interfaces, TMDS (HDMI and DVI) and Display Port (DP and DP++) on the same pins.

This means that it is possible to have Qseven® modules offering TMDS interface and other offering Display Port Interface. TMDS (HDMI) interface is also commonly native in ARM/RISC latest processors, while the Digital Display Interface (DP/DP++) is more common in x86 world. Moreover, the multimode Display Port interface (DP++) can also support HDMI/DVI displays through the use of external adapters.

For this reason, these two interfaces on the CQ7-A30 carrier board are not directly carried tout to a specific DP or HDMI connector. Instead, they are directly routed to an internal slot (PCI-e x16 type), so that it is possible to connect an additional expansion module for the implementation of the desired video interface (VA65 module, it is included in the "Cross Platform Development Kit 2.0". Please check par. 4.2 for further details).

! Please remember that CN19 uses a PCI-e x16 connector, but it is used to carry out DP++/TMDS interfaces, it is not used to realise a PCI-e interface. The compatibility with PCI-e x16 cards is only mechanical.

DP++/HDMI Slot- CN19

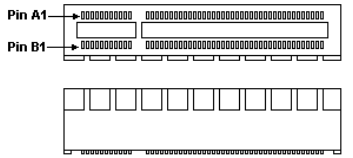
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_S	B1	A1	N.C.	
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
Not Connected	N.C.	B5	A5	N.C.	Not Connected
Not Connected	N.C.	B6	A6	N.C.	Not Connected
Power Ground	GND	B7	A7	N.C.	Not Connected
+3.3V Power Rail	+3.3V_S	B8	A8	N.C.	Not Connected
Not Connected	N.C.	B9	A9	+3.3V_S	+3.3V Power Rail
Not Connected	N.C.	B10	A10	+3.3V_S	+3.3V Power Rail
Not Connected	N.C.	B11	A11	PEG_RST#	Reset signal to the add-in card
Not Connected	N.C.	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	N.C.	Not Connected
TMDS Data Line 2+ or DP Data Line 0+	TMDS_LANE2+ / DP_LANE0+	B14	A14	N.C.	Not Connected

TMDS Data Line 2- or DP Data Line 0-	TMDS_LANE2- / DP_LANE0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	RSVD_144	Reserved pin (Differential pair)
HDMI I²C Control Clock Line	HDMI_CTRL_CLK	B17	A17	RSVD_146	Reserved pin (Differential pair)
Power Ground	GND	B18	A18	GND	Power Ground
TMDS Data Line 1+ or DP Data Line 1+	TMDS_LANE1+ / DP_LANE1+	B19	A19	N.C.	Not Connected
TMDS Data Line 1- or DP Data Line 1-	TMDS_LANE1- / DP_LANE1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	RSVD_132	Reserved pin (Differential pair)
Power Ground	GND	B22	A22	RSVD_134	Reserved pin (Differential pair)
TMDS Data Line 0+ or DP Data Line 2+	TMDS_LANE0+ / DP_LANE2+	B23	A23	GND	Power Ground
TMDS Data Line 0- or DP Data Line 2-	TMDS_LANE0- / DP_LANE2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	DP_AUX+	Display Port auxiliary channel +
Power Ground	GND	B26	A26	DP_AUX-	Display Port auxiliary channel -
TMDS Clock + or DP Data Line 3+	TMDS_CLK+ / DP_LANE3+	B27	A27	GND	Power Ground
TMDS Clock - or DP Data Line 3-	TMDS_CLK- / DP_LANE3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	DP_HDMI_HPD#	Display Port / HDMI Hot Plug Detect Input
Not Connected	N.C.	B30	A30	DP_HPD#	Display Port Hot Plug Detect Input
HDMI I²C Control Data Line	HDMI_CTRL_DAT	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	HDMI_CEC	Consumer Electronics Control (CEC) Line.
Not Connected	N.C.	B33	A33	N.C.	Not Connected
Not Connected	N.C.	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	N.C.	Not Connected
Power Ground	GND	B36	A36	N.C.	Not Connected
Not Connected	N.C.	B37	A37	GND	Power Ground
Not Connected	N.C.	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	N.C.	Not Connected
Power Ground	GND	B40	A40	N.C.	Not Connected
Not Connected	N.C.	B41	A41	GND	Power Ground
Not Connected	N.C.	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	N.C.	Not Connected
Power Ground	GND	B44	A44	N.C.	Not Connected

Not Connected	N.C.	B45	A45	GND	Power Ground
Not Connected	N.C.	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	N.C.	Not Connected
Not Connected	N.C.	B48	A48	N.C.	Not Connected
Power Ground	GND	B49	A49	GND	Power Ground
Not Connected	N.C.	B50	A50	N.C.	Not Connected
Not Connected	N.C.	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	N.C.	Not Connected
Power Ground	GND	B53	A53	N.C.	Not Connected
Not Connected	N.C.	B54	A54	GND	Power Ground
Not Connected	N.C.	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	N.C.	Not Connected
Power Ground	GND	B57	A57	N.C.	Not Connected
Not Connected	N.C.	B58	A58	GND	Power Ground
Not Connected	N.C.	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	N.C.	Not Connected
Power Ground	GND	B61	A61	N.C.	Not Connected
Not Connected	N.C.	B62	A62	GND	Power Ground
Not Connected	N.C.	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	N.C.	Not Connected
Power Ground	GND	B65	A65	N.C.	Not Connected
Not Connected	N.C.	B66	A66	GND	Power Ground
Not Connected	N.C.	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	N.C.	Not Connected
Power Ground	GND	B69	A69	N.C.	Not Connected
Not Connected	N.C.	B70	A70	GND	Power Ground
Not Connected	N.C.	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	N.C.	Not Connected
Power Ground	GND	B73	A73	N.C.	Not Connected
Not Connected	N.C.	B74	A74	GND	Power Ground

Not Connected	N.C.	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	N.C.	Not Connected
Power Ground	GND	B77	A77	N.C.	Not Connected
Not Connected	N.C.	B78	A78	GND	Power Ground
Not Connected	N.C.	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	N.C.	Not Connected
Not Connected	N.C.	B81	A81	N.C.	Not Connected
Not Connected	N.C.	B82	A82	GND	Power Ground

3.3.7 LVDS/eDP Slot



Similarly to HDMI and DP interfaces, the Qseven® specifications rel. 2.0 consider the possibility of having two other different video interfaces, LVDS and two embedded Display Ports (eDP) sharing the same pins.

This means that it is possible to have Qseven® modules offering LVDS interface and other offering embedded Display Port interfaces. For this reason, these two interfaces on the CQ7-A30 carrier board are not directly carried tout to specific LVDS or eDP connectors.

Instead, they are directly routed to an internal slot (PCI-e x8 type), so that it is possible to connect an additional expansion module for the implementation of the desired video interface (VA64 module, it is included in the “Cross Platform Development Kit 2.0”. Please check par. 4.1 for further details).

On the same connector, are also routed the signals, coming from the Qseven® connector, that are intended for the display and backlight management.

> **!** Please remember that CN20 uses a PCI-e x8 connector, but it is used to carry out LVDS/eDP interface, it is not used to realise a PCI-e interface. The compatibility with PCI-e add-on cards is only mechanical.

LVDS/eDP Slot- CN20					
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
+12V Power Rail	+12V_S	B1	A1	N.C.	
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
Not Connected	N.C.	B5	A5	N.C.	Not Connected
Not Connected	N.C.	B6	A6	N.C.	Not Connected

Power Ground	GND	B7	A7	N.C.	Not Connected
+3.3V Power Rail	+3.3V_S	B8	A8	N.C.	Not Connected
Not Connected	N.C.	B9	A9	+3.3V_S	+3.3V Power Rail
Not Connected	N.C.	B10	A10	+3.3V_S	+3.3V Power Rail
Not Connected	N.C.	B11	A11	LVDS_RST#	Reset signal to the add-in card
Not Connected	N.C.	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	LVDS_PPEN	LCD Panel Power Enable
LVDS or eDP primary channel pair 0 +	LVDS_A0+ / eDP0_TX0+	B14	A14	LVDS_BLEN	LCD Panel Backlight Enable
LVDS or eDP primary channel pair 0 -	LVDS_A0- / eDP0_TX0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	eDP0_HPD#	Primary eDP Hotplug detection
LVDS DisplayID Clock Line	LVDS_DID_CLK	B17	A17	eDP1_HPD#	Secondary eDP Hotplug detection
Power Ground	GND	B18	A18	GND	Power Ground
LVDS or eDP primary channel pair 1 +	LVDS_A1+ / eDP0_TX1+	B19	A19	N.C.	Not Connected
LVDS or eDP primary channel pair 1 -	LVDS_A1- / eDP0_TX1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	N.C.	Not Connected
Power Ground	GND	B22	A22	N.C.	Not Connected
LVDS or eDP primary channel pair 2 +	LVDS_A2+ / eDP0_TX2+	B23	A23	GND	Power Ground
LVDS or eDP primary channel pair 2 -	LVDS_A2- / eDP0_TX2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	LVDS_A_CLK+ / eDP0_AUX+	LVDS primary channel Clock + or eDP primary auxiliary channel +
Power Ground	GND	B26	A26	LVDS_A_CLK- / eDP0_AUX-	LVDS primary channel Clock + or eDP primary auxiliary channel -
LVDS or eDP primary channel pair 3 +	LVDS_A3+ / eDP0_TX3+	B27	A27	GND	Power Ground
LVDS or eDP primary channel pair 3 -	LVDS_A3- / eDP0_TX3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	LVDS_BLT_CTRL	LCD Panel brightness control (*)
Not Connected	N.C.	B30	A30	N.C.	Not Connected
LVDS DisplayID Data Line	LVDS_DID_DAT	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	N.C.	Not Connected
LVDS or eDP secondary channel pair 0 +	LVDS_B0+ / eDP1_TX0+	B33	A33	N.C.	Not Connected
LVDS or eDP secondary channel pair 0 -	LVDS_B0- / eDP1_TX0-	B34	A34	GND	Power Ground

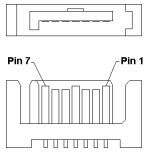
Power Ground	GND	B35	A35	N.C.	Not Connected
Power Ground	GND	B36	A36	N.C.	Not Connected
LVDS or eDP secondary channel pair 1 +	LVDS_B1+ / eDP1_TX1+	B37	A37	GND	Power Ground
LVDS or eDP secondary channel pair 1 -	LVDS_B1- / eDP1_TX1-	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	LVDS_B_CLK+ / eDP1_AUX+	LVDS secondary channel Clock + or eDP secondary auxiliary channel +
Power Ground	GND	B40	A40	LVDS_B_CLK- / eDP1_AUX-	LVDS secondary channel Clock - or eDP secondary auxiliary channel -
LVDS or eDP secondary channel pair 2 +	LVDS_B2+ / eDP1_TX2+	B41	A41	GND	Power Ground
LVDS or eDP secondary channel pair 2 -	LVDS_B2- / eDP1_TX2-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	N.C.	Not Connected
Power Ground	GND	B44	A44	N.C.	Not Connected
LVDS or eDP secondary channel pair 3 +	LVDS_B3+ / eDP1_TX3+	B45	A45	GND	Power Ground
LVDS or eDP secondary channel pair 3 -	LVDS_B3- / eDP1_TX3-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	N.C.	Not Connected
Not Connected	N.C.	B48	A48	N.C.	Not Connected
Power Ground	GND	B49	A49	GND	Power Ground

(*) LVDS_BLT_CTRL signal will be available only when SW11 switch #1 is set to OFF position.

3.3.8 SATA connectors

SATA #0 M 7p Connector - CN11	
Pin	**Signal**
1	GND
2	SATA0_Tx+
3	SATA0_Tx-
4	GND
5	SATA0_Rx-
6	SATA0_Rx+
7	GND

For the connection of external Mass Storage Devices, there is a standard male SATA connector, CN11.



This connector carries out directly SATA port#0 signals coming from Qseven® module's connector.

Please notice that SATA connectors will work only in case the Qseven® module carries out SATA Channel #0 on Qseven® connector (pins 29, 31, 35, 37). In case the Qseven® module used doesn't have these signals connected, then this connector will not be usable.

Here following the signals related to SATA interface:

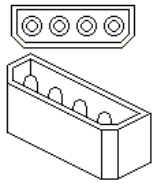
SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

The SATA channel #0 is switched with mSATA Slot (CN8). The switching is automatic, depending on the presence or not of an mSATA device in the dedicated slot. This means that if a mSATA disk is plugged in the slot CN8, then the connector CN11 will not work.

SATA Power Connector - CN10	
Pin	**Signal**
1	+12V_S
2	GND
3	GND
4	+5V_S

A dedicated power connector, CN 10, can be used to give supply to external Hard Disks (or Solid State Disks) connected to the SATA male connector.



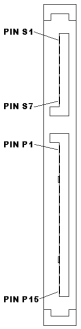
The dedicated power connector is a 4-pin male connector, type TKP p/n 4070l-04 or equivalent, with pinout shown in the table on the left (it is the standard HDD Power connector).

Mating connector: TKP 8851-04 crimp housing with TKP 8851T crimp terminals.

An adapter cable for powering SATA disks from this connector is also contained inside the "Cross Platform Development Kit 2.0". Please check par. 4.3 for further details.

SATA #1 F 7+15p connector - CN9			
Pin	**Signal**	**Pin**	**Signal**
S1	GND	P5	GND
S2	SATA1_TX+	P6	GND
S3	SATA1_TX-	P7	+5V_S
S4	GND	P8	+5V_S
S5	SATA1_RX-	P9	+5V_S
S6	SATA1_RX+	P10	GND
S7	GND	P11	GND
P1	+3.3V_S	P12	GND
P2	+3.3V_S	P13	+12V_S
P3	+3.3V_S	P14	+12V_S
P4	GND	P15	+12V_S

A second SATA port is available on SATA female connector CN9, a standard female 22 poles SATA connector, which can be used also for direct powering of SATA Hard Disk Drive.



Connector used is type MOLEX p/n 87779-1001 or equivalent, with pinout shown in the dedicated table on the left.

This connector carries out directly SATA port#1 signals coming from Qseven® module's connector.

Please notice that SATA connectors will work only in case the Qseven® module carries out SATA Channel #1 on Qseven® connector (pins 30, 32, 36, 38). In case the Qseven® module used doesn't have these signals connected, then this connector will not be usable.

Here following the signals related to SATA interface:

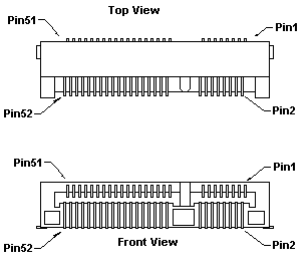
SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

3.3.9 mSATA slot

mSATA Slot - CN8			
Pin	**Signal**	**Pin**	**Signal**
1	N.C.	2	+3.3V_S
3	N.C.	4	GND
5	N.C.	6	N.C.
7	N.C.	8	N.C.
9	GND	10	N.C.
11	N.C.	12	N.C.
13	N.C.	14	N.C.
15	GND	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	GND	22	N.C.
23	SATA0_RX+	24	+3.3V_S
25	SATA0_RX-	26	GND
27	GND	28	N.C.
29	GND	30	N.C.
31	SATA0_TX-	32	N.C.
33	SATA0_TX+	34	GND
35	GND	36	N.C.
37	GND	38	N.C.
39	+3.3V_S	40	GND
41	+3.3V_S	42	N.C.
43	GND	44	N.C.
45	N.C.	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	mSATA_DET#	52	+3.3V_S

To increase mass storage possibilities, it is possible to use mSATA Solid State Disks, using the dedicate connector, CN8, which is a standard 52pin miniPCI Express connector, type TE 1775861-4 or equivalent, H=4.0mm, with the pinout shown in the table on the left.



Signals carried to mSATA slot are the following:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA_RX+/SATA0_RX-: Serial ATA Channel # Receive differential pair.

mSATA_DET#: mSATA Presence Detection pin. This signal is driven low by mSATA disks plugged in the CN8 slot. It is used to switch the SATA Channel #0 between the mSATA slot and the SATA Connector CN11 (when an mSATA disk is plugged into CN8, then CN11 will be disabled).

When a mSATA disk is plugged into the slot, a red LED (D2) will light.

Please be aware that mSATA slot will work only in case the Qseven® module carries out SATA Channel #0 on Qseven® connector (pins 29, 31, 35, 37). In case the Qseven® module used doesn't have these signals connected, then this slot will not be usable.

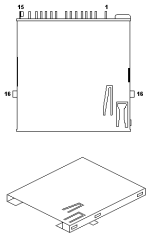
A red LED, D25, is located on the PCB near the mSATA slot, between the SD Card and the SIM Card slots; it will blink to signal activity (i.e. data transfers) on one or both the SATA Channels (SATA connectors and/or mSATA Slot).

3.3.10 SD card slot

SD Card Slot - CN36			
Pin	**Signal**	**Pin**	**Signal**
1	SDIO_DAT2	9	SDIO_CLK#
2	SDIO_DAT3	10	SDIO_DAT6
3	SDIO_DAT4	11	GND
4	SDIO_CMD	12	SDIO_DAT7
5	SDIO_DAT5	13	SDIO_DAT0
6	SDIO_CD#	14	SDIO_DAT1
7	GND	15	SDIO_WP
8	+3.3V_S	16	GND

Since Qseven® standard contemplates signals for Secure Digital Input/Output and MultiMedia Cards, on CQ7-A30 carrier board there is also a socket, for the use of standard SD or MMC cards, to be used as Mass Storage Device and/or Boot Device (if the Qseven® used with this carrier board implements this functionality).

Please refer to the User Manual of the used Qseven® module for information about Card types supported by the chipset.



The connector used is a combo SD/MMC slot, push-push type, H=3.2 mm., type PROCONN SDSN13-A0-0005 or equivalent. Pinout here reported is related only to signal routing on specific connector, internally the pin-out is the same of any standard SD or MMC 4.0 card.

For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

Signals related to SDIO/MMC cards are the following:

SDIO_CD#: Card Detect Input.

SDIO_CLK: SD Clock Line (output).

SDIO_CMD: Command/Response bidirectional line.

SDIO_DAT[0÷7]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode. SDIO_DAT[5÷7] signals are also required for 8-bit communication mode.

SDIO_WP: SD Write Protect Input. This signal denotes the state of the write-protect tab on SD cards.

A red LED (D28) is placed near the SD Card Slot. It will blink to signal activity (i.e. data transfers) on the SDIO interface.

3.3.11 Audio Interface

Qseven® modules can have three different audio standard interfaces (AC'97, HD audio, I2S) on the same pins.

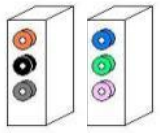
Commonly, x86 modules offer HD Audio interface, where I2S and AC'97 are more common for ARM/RISC world.

The modules offering HD Audio interface can use the HD Audio Codec (Realtek ALC888) which is available on board.

This codec manages two triple Audio jacks, type LOTES p/n ABA-JAK-028-K08 (Orange / Black / Grey) and ABA-JAK-028-K07 (light blue / light green / pink) or equivalent.

Triple Audio Jack 1- CN21	
Color	**Signal**
Orange	Center + Subwoofer speakers
Black	Rear Surround Out (Left + Right)
Grey	Side Surround Out (Left + Right)

Triple Audio Jack 2- CN22	
Color	**Signal**
Light Blue	Line IN (Left + Right)
Light Green	Front OUT (Left + Right)
Pink	MIC IN (Left + Right)



Integrated HD Audio Codec of CQ7-A30 Carrier also offers the possibility of connecting high quality digital audio devices, using S/P-DIF optical connection.

At this purpose, on board there is a Fiber Optic POF connector, CN23, Toslink type, model FOXCONN 2F11TC1-EM92-4F or equivalent. This connector can be used for S/PDIF Audio output.

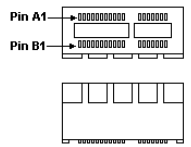
S/PDIF Input Connector- CN51	
Pin	**Signal**
1	GND
2	+5V_S
3	S/PDIF_IN

It is also available a connector, type TE p/n 103669-2 or equivalent, for S/PDIF Input connection.

Mating connector TE p/n 487526-2 or equivalent, with contacts TE series 487117 or 487406.

Since the Qseven® module can offer different audio interfaces, it is given the possibility of using different audio Codecs by plugging an add-on audio card on dedicated slot CN24, which uses a connector usually used for PCI-e x1 add-on cards.

If the add-on card is developed according to the electrical requirements of PCI-e cards, i.e. with pin A1 short-circuited with pin B17 (PRSNT#), then plugging the audio add-on card the audio signals coming from Qseven® card edge connector will be automatically switched to connector CN24, and not to the HD Audio Codec. This also means that connectors CN21, CN22, CN23 and CN51 will not work when an audio add-on card is plugged in CN24 slot.



! Please remember that CN24 uses a PCI-e x1 connector, but it is used to carry out HD / AC'97 / I2S audio interface, it is not used to realise a PCI-e interface. The compatibility with PCI-e add-on cards is only mechanical and electrical, not functional.

Audio Interface Slot CN24					
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
+12V Power Rail	+12V_S	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
General Purpose I²C Bus Clock line	GP0_I2C_CK	B5	A5	AUDIO_BCLK	HD/AC'97 24MHz Serial Bit Clock or I2S Serial Data Clock signal
General Purpose I²C Bus Data line	GP0_I2C_DAT	B6	A6	AUDIO_SDO	Audio Serial Data Output signal
Power Ground	GND	B7	A7	AUDIO_SDIN	Audio Serial Data Input signal
+3.3V Power Rail	+3.3V_S	B8	A8	AUDIO_SYNC	HD/AC'97 Serial Bus Synchronization or I2S Word Select signal
Audio Reset signal	AUDIO_RST#	B9	A9	+3.3V_S	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_A	B10	A10	+3.3V_S	+3.3V Power Rail
Not Connected	N.C.	B11	A11	N.C.	Not Connected
Speaker Signal Output	AUDIO_SPKR (*)	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	N.C.	Not Connected
Not Connected	N.C.	B14	A14	N.C.	Not Connected
Not Connected	N.C.	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	N.C.	Not Connected
Hot Plug presence detect	AUDIO_PRSNT2#	B17	A17	N.C.	Not Connected
Power Ground	GND	B18	A18	GND	Power Ground

(*) AUDIO_SPKR signal will be available only when SW11 switch #3 is set to OFF position.

3.3.12 PCI-express slots

CQ7-A30 board offer a possibility of expansion through a standard PCI-e x16 card edge connector, type TE p/n 2-1612163-4 or equivalent, with the pinout shown in the following table.

On this slot, are carried out the four PCI express lanes coming from Qseven® Card edge connector. Please be aware that availability of all four PCI express lanes depends on the Qseven® module used.

Please check the User Manual of the Qseven® module used for details about the availability of these lanes.

It is also recommended to check that User Manual to see if these PCI-express lanes can be used in a grouped configuration, i.e. if they can be used in PCI-e x4 mode, in 2 x PCI-e x2, in 1 x PCI- e x2 + 2 x PCI-e x1, or if they must be strictly used in single lane configuration (i.e., four independent PCI-e x1 lanes).

PCI-e x16 Slot- CN14					
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
+12V Power Rail	+12V_S	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line	SMB_CLK	B5	A5	JTAG2	TCK, tied to GND with 4K7Ω resistor
SM Bus Data line	SMB_DAT	B6	A6	JTAG3	TDI, tied to +3.3V_S with 4K7Ω resistor
Power Ground	GND	B7	A7	JTAG4	Test Data Out, not connected
+3.3V Power Rail	+3.3V_S	B8	A8	JTAG5	TMS, tied to +3.3V_S with 4K7Ω resistor
TRST#, tied to GND with 4K7Ω resistor	JTAG1	B9	A9	+3.3V_S	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_A	B10	A10	+3.3V_S	+3.3V Power Rail
Wake signal for link reactivation	PCIE_WAKE#	B11	A11	PEG_RST#	Reset signal to the add-in card
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PEG_CLK_REF+	PCI-e x16 slot reference clock lane +
PCI-e lane #0 Transmitter +	PCIE0_TX+	B14	A14	PEG_CLK_REF-	PCI-e x16 reference clock lane -
PCI-e lane #0 Transmitter -	PCIE0_TX-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE0_RX+	PCI-e lane #0 Receiver +
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B17	A17	PCIE0_RX-	PCI-e lane #0 Receiver -
Power Ground	GND	B18	A18	GND	Power Ground

PCI-e lane #1 Transmitter +	PCIE1_TX+	B19	A19	RSVD	Not connected
PCI-e lane #1 Transmitter -	PCIE1_TX-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE1_RX+	PCI-e lane #1 Receiver +
Power Ground	GND	B22	A22	PCIE1_RX-	PCI-e lane #1 Receiver -
PCI-e lane #2 Transmitter +	PCIE2_TX+	B23	A23	GND	Power Ground
PCI-e lane #2 Transmitter -	PCIE2_TX-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE2_RX+	PCI-e lane #2 Receiver +
Power Ground	GND	B26	A26	PCIE2_RX-	PCI-e lane #2 Receiver -
PCI-e lane #3 Transmitter +	PCIE0_TX+	B27	A27	GND	Power Ground
PCI-e lane #3 Transmitter -	PCIE0_TX-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE3_RX+	PCI-e lane #3 Receiver +
Not Connected	RSVD	B30	A30	PCIE3_RX-	PCI-e lane #3 Receiver -
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not connected
Not Connected	N.C.	B33	A33	RSVD	Not connected
Not Connected	N.C.	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	N.C.	Not connected
Power Ground	GND	B36	A36	N.C.	Not connected
Not Connected	N.C.	B37	A37	GND	Power Ground
Not Connected	N.C.	B38	A38	GND	Power Ground
Power Ground	GND	B39	A39	N.C.	Not connected
Power Ground	GND	B40	A40	N.C.	Not connected
Not Connected	N.C.	B41	A41	GND	Power Ground
Not Connected	N.C.	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	N.C.	Not connected
Power Ground	GND	B44	A44	N.C.	Not connected
Not Connected	N.C.	B45	A45	GND	Power Ground
Not Connected	N.C.	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	N.C.	Not connected
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B48	A48	N.C.	Not connected

Power Ground	GND	B49	A49	GND	Power Ground
Not Connected	N.C.	B50	A50	N.C.	Not connected
Not Connected	N.C.	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	N.C.	Not connected
Power Ground	GND	B53	A53	N.C.	Not connected
Not Connected	N.C.	B54	A54	GND	Power Ground
Not Connected	N.C.	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	N.C.	Not connected
Power Ground	GND	B57	A57	N.C.	Not connected
Not Connected	N.C.	B58	A58	GND	Power Ground
Not Connected	N.C.	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	N.C.	Not connected
Power Ground	GND	B61	A61	N.C.	Not connected
Not Connected	N.C.	B62	A62	GND	Power Ground
Not Connected	N.C.	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	N.C.	Not connected
Power Ground	GND	B65	A65	N.C.	Not connected
Not Connected	N.C.	B66	A66	GND	Power Ground
Not Connected	N.C.	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	N.C.	Not connected
Power Ground	GND	B69	A69	N.C.	Not connected
Not Connected	N.C.	B70	A70	GND	Power Ground
Not Connected	N.C.	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	N.C.	Not connected
Power Ground	GND	B73	A73	N.C.	Not connected
Not Connected	N.C.	B74	A74	GND	Power Ground
Not Connected	N.C.	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	N.C.	Not connected
Power Ground	GND	B77	A77	N.C.	Not connected
Not Connected	N.C.	B78	A78	GND	Power Ground

Not Connected	N.C.	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	N.C.	Not connected
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B81	A81	N.C.	Not connected
Not Connected	RSVD	B82	A82	GND	Power Ground

Please be aware that PCI-e management on CQ7-A30 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

The single PCI-express lanes that come out from Qseven® card edge connector can be alternatively routed to three (3) single PCI-e x1 lanes and one miniPCI-e Slot. The switching between the single PCI-e x 16 slot and the different connectors is made using jumper JP1, which is a two-way P 2.54mm jumper.

JP1 position	PCI-e lanes routing:			
	Lane #0	Lane #1	Lane #2	Lane #3
Not inserted	miniPCI-e slot CN18	PCI-e x1 slot CN15	PCI-e x1 slot CN16	PCI-e x1 slot CN17
Inserted	PCI-e x 16 slot CN14			

According to the table above reported, when JP1 is not inserted, then three PCI-e x1 slots are singularly enabled.

PCI-e x1 Slot #1 - CN15					
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
+12V Power Rail	+12V_S	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line	SMB_CLK	B5	A5	N.C.	Not connected
SM Bus Data line	SMB_DAT	B6	A6	N.C.	Not connected
Power Ground	GND	B7	A7	N.C.	Not connected
+3.3V Power Rail	+3.3V_S	B8	A8	N.C.	Not connected
Not connected	N.C.	B9	A9	+3.3V_S	+3.3V Power Rail

+3.3V Auxiliary Power Rail	+3.3V_A	B10	A10	+3.3V_S	+3.3V Power Rail
Wake signal for link reactivation	PCIE_WAKE#	B11	A11	PCIE1_RST#	Reset signal to the add-in card
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIE_CLK1_REF+	PCI-e #1 reference clock lane +
PCI-e lane #1 Transmitter +	PCIE1_TX+	B14	A14	PCIE_CLK1_REF-	PCI-e #1 reference clock lane -
PCI-e lane #1 Transmitter -	PCIE1_TX-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE1_RX+	PCI-e lane #1 Receiver +
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B17	A17	PCIE1_RX-	PCI-e lane #1 Receiver -
Power Ground	GND	B18	A18	GND	Power Ground

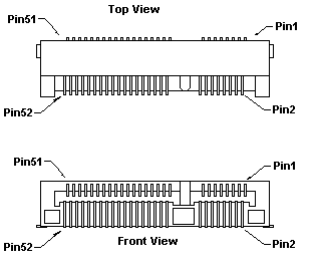
PCI-e x1 Slot #2 CN16

Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_S	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line	SMB_CLK	B5	A5	N.C.	Not connected
SM Bus Data line	SMB_DAT	B6	A6	N.C.	Not connected
Power Ground	GND	B7	A7	N.C.	Not connected
+3.3V Power Rail	+3.3V_S	B8	A8	N.C.	Not connected
Not connected	N.C.	B9	A9	+3.3V_S	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_A	B10	A10	+3.3V_S	+3.3V Power Rail
Wake signal for link reactivation	PCIE_WAKE#	B11	A11	PCIE2_RST#	Reset signal to the add-in card
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIE_CLK2_REF+	PCI-e #2 reference clock lane +
PCI-e lane #2 Transmitter +	PCIE2_TX+	B14	A14	PCIE_CLK2_REF-	PCI-e #2 reference clock lane -
PCI-e lane #2 Transmitter -	PCIE2_TX-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE2_RX+	PCI-e lane #2 Receiver +
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B17	A17	PCIE2_RX-	PCI-e lane #2 Receiver -
Power Ground	GND	B18	A18	GND	Power Ground

PCI-e x1 Slot #3 CN17					
Description	**Pin name**	**Pin nr.**	**Pin nr.**	**Pin name**	**Description**
+12V Power Rail	+12V_S	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_S	B2	A2	+12V_S	+12V Power Rail
+12V Power Rail	+12V_S	B3	A3	+12V_S	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line	SMB_CLK	B5	A5	N.C.	Not connected
SM Bus Data line	SMB_DAT	B6	A6	N.C.	Not connected
Power Ground	GND	B7	A7	N.C.	Not connected
+3.3V Power Rail	+3.3V_S	B8	A8	N.C.	Not connected
Not connected	N.C.	B9	A9	+3.3V_S	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_A	B10	A10	+3.3V_S	+3.3V Power Rail
Wake signal for link reactivation	PCIE_WAKE#	B11	A11	PCIE3_RST#	Reset signal to the add-in card
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIE_CLK3_REF+	PCI-e #3 reference clock lane +
PCI-e lane #3 Transmitter +	PCIE3_TX+	B14	A14	PCIE_CLK3_REF-	PCI-e #3 reference clock lane -
PCI-e lane #3 Transmitter -	PCIE3_TX-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE3_RX+	PCI-e lane #3 Receiver +
Hot Plug presence detect (needed to enable clock)	PRSNT#2	B17	A17	PCIE3_RX-	PCI-e lane #3 Receiver -
Power Ground	GND	B18	A18	GND	Power Ground

3.3.13 miniPCI-express slot

miniPCI-e Slot - CN18			
Pin	**Signal**	**Pin**	**Signal**
1	PCIE_WAKE#	2	+3.3V_A
3	N.C.	4	GND
5	N.C.	6	+1.5V_S
7	mPCIE_CLOCK_REQUEST#	8	UIM_PWR
9	GND	10	UIM_DATA
11	mPCIE_CLK-	12	UIM_CLK
13	mPCIE_CLK+	14	UIM_RESET
15	GND	16	UIM_SPU
17	N.C.	18	GND
19	N.C.	20	W_DISABLE#
21	GND	22	mPCIE_RST#
23	PCIE0_RX-	24	+3.3V_A
25	PCIE0_RX+	26	GND
27	GND	28	+1.5V_S
29	GND	30	SMB_CLK
31	PCIE0_TX-	32	SMB_DAT
33	PCIE0_TX+	34	GND
35	GND	36	USB_mPCIE-
37	GND	38	USB_mPCIE+
39	+3.3V_A	40	GND
41	+3.3V_A	42	LED_WWAN0#
43	GND	44	LED_WLAN0#
45	N.C.	46	LED_WPAN0#
47	N.C.	48	+1.5V_S
49	N.C.	50	GND
51	N.C.	52	+3.3V_A



To add communications functionality, or other features not already available, it is possible to use Half-/ Full-size mini-PCI Express cards, using the dedicate connector, CN18, which is a standard 52pin miniPCI Express connector, type LOTES AAA-PCI-047-K01 or equivalent, H=9.0mm, with the pinout shown in the table on the left.

CQ7-A30 carrier board allows inserting both Half-mini and Full-mini PCI express cards. Support for both form factors is ensured by the possibility, for the customer, of moving the mechanical latch in the position necessary to support Half-miniPCI-e cards or Full-miniPCI-e cards.

On the slot are also available the signals for interfacing to miniSIM cards, so that it is possible to use miniPCI Express modems.

As explained in the previous paragraph, PCI-e lane is available on CN18 when jumper JP1 is not inserted, otherwise PCI-e lane #0 would be routed to PCI-e x16 slot CN14.

Signals carried to miniPCI-express slot are the following:

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair.

mPCIE_CLK+ / mPCIE_CLK-: Reference Clock for miniPCI express slot, Differential Pair.

PCIE_WAKE#: Board's Wake Input, it must be externally driven by the miniPCI-e module inserted in the slot when it requires waking up the system.

mPCIE_RST#: Reset Signal derived from those sent from Qseven® module to all devices available on the board. It is a 3.3V active-low signal.

mPCIE_CLOCK_REQUEST# PCI Express Clock Request Input. This signal shall be driven correctly by any module inserted in the miniPCI express slot, in order to ensure that the PCI-e clock buffer available on the carrier board makes available the reference clock for the miniPCI-e slot.

SMB_CLK: SM Bus control clock line for System Management, managed by the Qseven® module.

SMB_DATA: SM Bus control data line for System Management, managed by the Qseven®

module.

USB_mPCIE+ / USB_mPCIE-: USB Port #2 differential pair, switched to the miniPCI-e slot by using the SW6 dedicated switch #3. Please check par 3.3.5for details about switch SW6 setting.

W_DISABLE#: Wireless disable. This signal is HW controlled through the jumper JP6, which is a two-way P 2.54mm jumper.

JP6 position	Wireless operations
Not inserted	WiFi operations allowed
Inserted	WiFi disabled

UIM_PWR: Power line for UIM module.

UIM_DATA: Bidirectional Data line between miniPCI-express card and UIM module.

UIM_CLK: Clock line, output from miniPCI-express card to the UIM module.

UIM_RESET: Reset signal line, sent from miniPCI-express card to the UIM module.

UIM_SPU: UIM Standard or Proprietary Use signal.

Please be aware that all signals related to User Identity Modules are managed directly by the miniPCI-express card circuitry, they don't involve neither carrier board's nor Qseven® module's management. The CQ7-A30 carrier board embeds only clamping diodes for ESD protection on UIM signal and voltage lines.

Three SMT RED LEDs are present near this Mini PCI-Express Card Slot to show the presence of an eventual Wi-Fi PCI-Express Card inserted in the slot. These LEDs can work only if the Wi-Fi Mini PCI Express Card you are using supports and drives them opportunely.

Red LED D3: Wireless_WAN #0 present (cellular data, like GSM/GPRS/UMTS)

Red LED D4: Wireless_LAN #0 present (for wireless networks 802.11b/g/a)

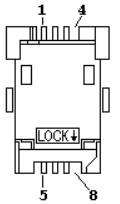
Red LED D5: Wireless_PAN #0 present (Bluetooth).

3.3.14 miniSIM Card Slot

miniSIM Card Slot - CN52			
Pin	Signal	Pin	Signal
1	UIM_PWR	5	GND
2	UIM_RESET	6	UIM_SPU
3	UIM_CLK	7	UIM_DATA
4	1KΩ Pull-down to GND	8	GND

Interfaced to miniPCI express slot CN18, as already told in previous paragraph, there is a miniSIM Card Slot, to be used in conjunction with miniPCI-e modems. Here it is possible to insert the SIM card provided by any telecommunication operator for the connection to their network.

The socket is type FRAMATOME p/n 7312S0815X19LF or equivalent, with the pinout shown in the table on the left.



3.3.15 Serial ports

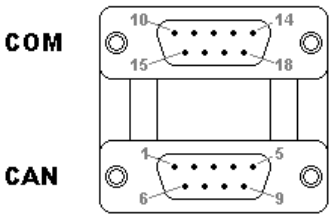
Serial ports are a kind of interface that is much common in electronic devices, especially in industrial application.

Considering this, on CQ7-A30 there are many possibilities for connecting serial ports, so that each customer can study their application in its own design.

Qseven® COM (RS-232) DB9 connector CN26

Pin	Signal	Pin	Signal
10	N.C.	15	N.C.
11	RxD_0	16	RTS_0#
12	TxD_0	17	CTS_0#
13	N.C.	18	N.C.
14	GND		

First possibility, it is given by the serial port that is offered natively on Qseven® card edge connector. This interface (eventually managed by the processor/chipset of the Qseven® module used), is at TTL electrical level, i.e. it cannot be used directly for the connection of common PCs or consumer peripherals.



For this reason, on the carrier board there is a dedicated transceiver, which makes the serial port available in standard RS-232 mode. It is made externally available on a double DB9 male connector, with the pinout shown in the table on the left (standard for COM ports on DB9 male connectors). On the CN26 combo connector, the DB9 male connector dedicated to the Serial Port managed directly by the Qseven® module is the upper one (the lower one is dedicated to the CAN port, see par. 3.3.16)

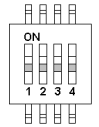
Please remember that RS-232 signals RxD_0, TxD_0, RTS_0# and CTS_0# are obtained from signals UART0_RX, UART0_TX, UART0_RTS# and UART0_CTS# coming out from Qseven® card edge connector. If the Qseven® module used doesn't support the UART interface in those pins, then serial port #0 on connector CN29 will not be usable.

Other serial port interfaces are offered by the LPC to UART bridge XR28V384IM48, which allows the implementation of four further serial ports. All of these serial ports are made available through two combo DB9 male + male connectors, CN28 and CN29, with the pinout shown in the table in the next page.

Considering the serial ports managed by this bridge, COM ports #1 and #4 are offered with RS-232 only interface, while COM#2 and COM#3 are managed using a multistandard transceiver, which allows using them in RS-232, RS-422 or RS-485 mode.

SW12 Switch	ON Position	OFF Position
1	COM#2 in RS-232 mode	COM#2 in RS-485 mode
2	COM#2 in RS-485 Half Duplex mode	COM#2 in RS-485 Full Duplex mode (RS-422)
3	COM#3 in RS-232 mode	COM#3 in RS-485 mode
4	COM#3 in RS-485 Half Duplex mode	COM#3 in RS-485 Full Duplex mode (RS-422)

The selection of working mode is made using dedicated Dip switch SW6, with the meaning shown in the table on the left.



! Please be aware that only Qseven® modules offering LPC interface will be able to drive correctly the serial ports available on connectors CN28 and CN29.

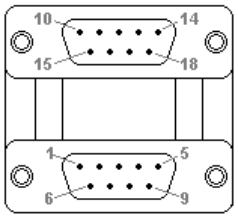
Furthermore, it is necessary that the LPC-to-UART Bridge is supported by module's BIOS / BSP.

XR28V384 COM port #2 connector - CN29			
Pin	Signal RS-232 mode	Signal RS-485 Full Duplex mode	Signal RS-485 Half Duplex mode
1	N.C.	N.C.	N.C.
2	RxD_2	RX_2+	N.C.
3	TxD_2	TX_2-	RX_2-/TX_2-
4	N.C.	N.C.	N.C.
5	GND	GND	GND
6	N.C.	N.C.	N.C.
7	RTS_2#	TX_2+	RX_2+/TX_2+
8	CTS_2#	RX_2-	N.C.
9	N.C.	N.C.	N.C.

XR28V384 COM port #3 connector - CN29			
Pin	Signal RS-232 mode	Signal RS-485 Full Duplex mode	Signal RS-485 Half Duplex mode
10	N.C.	N.C.	N.C.
11	RxD_3	RX_3+	N.C.
12	TxD_3	TX_3-	RX_3-/TX_3-
13	N.C.	N.C.	N.C.
14	GND	GND	GND
15	N.C.	N.C.	N.C.
16	RTS_3#	TX_3+	RX_3+/TX_3+
17	CTS_3#	RX_3-	N.C.
18	N.C.	N.C.	N.C.

XR28V384 COM port #1 connector - CN28	
Pin	Signal
1	DCD_1#
2	RxD_1
3	TxD_1
4	DTR_1#
5	GND
6	DSR_1#
7	RTS_1#
8	CTS_1#
9	RI_1#

XR28V384 COM port #4 connector - CN28	
Pin	Signal
10	DCD_4#
11	RxD_4
12	TxD_4
13	DTR_4#
14	GND
15	DSR_4#
16	RTS_4#
17	CTS_4#
18	RI_4#

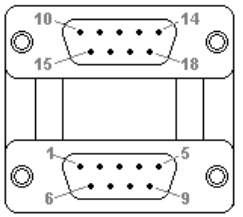


W83627DHG RS-232 COM port #1 connector - CN12			
Pin	Signal	Pin	Signal
1	W_DCD_1#	6	W_DSR_1#
2	W_RxD_1	7	W_RTS_1#
3	W_TxD_1	8	W_CTS_1#
4	W_DTR_1#	9	W_RI_1#
5	GND		

W83627DHG RS-232 COM port #2 connector - CN12			
Pin	Signal	Pin	Signal
10	W_DCD_2#	15	W_DSR_2#
11	W_RxD_2	16	W_RTS_2#
12	W_TxD_2	17	W_CTS_2#
13	W_DTR_2#	18	W_RI_2#
14	GND		

Finally, other two serial port interfaces are offered by the LPC SuperI/O W83627DHG.

These serial ports are carried out externally through two dedicated RS-232 transceiver, and are available on connector CN12, which is another combo DB9 male + male connector, with the standard pinout shown in the table on the left.

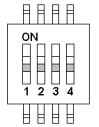


! Only Qseven® modules offering LPC interface will be able to drive correctly the serial ports available on conenctors CN12. Furthermore, it is necessary that the LPC SuperI/O is supported by module's BIOS / BSP.

Please remember that the serial ports offered by the LPC-to-UART bridge XR28V384 and/or those offered by the LPC SuperI/O W83627DHG will be available only in case that the Qseven® module used is able to manage these devices. It is also possible that the module used is able to manage both of them at the same time.

In order to avoid address conflicts between the two devices, it is available onboard a dedicated Dip Switch, SW2, for single device enabling/disabling and address selection.

SW2 Switch	ON Position	OFF Position
1	W83627DHG enabled	W83627DHG disabled
2	W83627 at address 4Eh	W83627 at address 2Eh
3	XR28V384 enabled	XR28V384 disabled
4	XR28V384 at address 4Eh	XR28V384 at address 2Eh



! In order to avoid address conflicts, when both W83627DHG and XR28V384 are anabled, SW2 switches #2 and #4 must not be in the same position at the same time (i.e, they must not be simultaneously ON or simultaneously OFF).

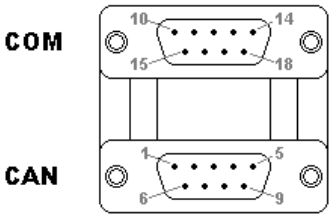
3.3.16 CAN Interface

CAN DB9 connector CN26			
Pin	**Signal**	**Pin**	**Signal**
1	N.C.	6	GND
2	CAN_L	7	CAN_H
3	GND	8	N.C.
4	N.C.	9	CAN_VDD
5	GND		

According to Qseven® specifications, the modules can optionally offer a CAN interface, since many architectures offer this kind of interface natively.

For this reason, on CQ7-A30 carrier board there is a CAN transceiver, which allows the system to be interfaced directly to any CAN Network.

The interface is available on the lower DB9 male of the CN26 combo connector (the upper one is dedicated to the COM coming from the Qseven® module, see par. 3.3.15)



CAN_H: High Level CAN Bus line

CAN_L: Low level CAN Bus line

CAN_VDD: Power output for CAN Bus line. Please check JP10 description.

JP11 position	120Ω CAN Termination
Not Inserted	Termination disconnected
Inserted	Termination present

CAN interface can optionally be terminated with a 120Ω Resistor, in case CQ7-A30 carrier is at one of the extremities of the CAN line. To enable this termination, is necessary to use jumper JP6, which is a standard pin header, P2.54mm, 1x2 pin, according to the table on the left.

It could also be possible to use the CAN interface directly at TTL level, i.e. using the signals that come out directly from Qseven® card edge connector.

CAN TTL pin header - CN25			
Pin	**Signal**	**Pin**	**Signal**
1	CAN_VDD	2	CAN0_RX (*)
3	N.C.	4	CAN0_TX (*)
5	GND	6	+3.3V_S
7	N.C.	8	GND
	GND	10	N.C.

The related signals are carried out an internal 10-pin standard male pin header (CN32), p 2.54 mm, 10 pin, dual row, h= 6mm, with the pinout shown in the table on the left.

CAN0_TX: CAN Transmit Output for CAN Bus Channel.

CAN0_RX: CAN Receive Input for CAN Bus Channel.

(*) As a factory default, these signals are not connected on this connector, since they are used to drive the CAN transceiver which manages the CN26 connector. If it is necessary to use CAN at TTL level on CN25, instead of using the CAN interface on CN26, then it is possible to reconnect CAN0_RX and CAN0_TX on CN25, leaving CN26 not working. Please contact SECO for information on this rework.

JP10 position	CAN_VDD Voltage
1-2	+12V_S
2-3	+5V_S

CAN_VDD: Power output for CAN Bus line (also available on connector CN26). The power rail that has to be used to supply the CAN Bus line can be selected by using jumper JP10, which is a standard pin header, P2.54mm, 1x3 pin.

3.3.17 PS/2 Mouse + Keyboard Pin header

PS/2 Mouse + Keyboard Pin header - CN13	
Pin	**Signal**
1	KEYB_DAT
2	N.C.
3	MS_DAT
4	GND
5	$+5V_{PS2}$
6	KEYB_CLK
7	MS_CLK

On CQ7-A30 carrier board is also available a single row, 7-pin p2.54mm pin header, for the connection of legacy PS/2 peripherals (mouse and/or keyboard), managed by the LPC Super I/O W83627DHG (the same that manages the serial ports available on combo connector CN12).

KEYB_DAT: PS/2 data line for keyboard connection

KEYB_CLK: PS/2 clock line for keyboard connection

MS_DAT: PS/2 data line for mouse connection

MS_CLK: PS/2 clock line for mouse connection

! Please be aware that the support for legacy PS/2 peripherals is not provided for by Qseven® specifications. This means that the working of PS/2 interface depends strongly on the BIOS of the Qseven® module used, which might not manage this interface, even if it supports correctly the W83627DHG SuperI/O. A customised BIOS could be necessary in order to enable PS/2 support.

3.3.18 LPC/GPIO Pin header

LPC/GPIO Pin Header - CN3			
Pin	**Signal**	**Pin**	**Signal**
1	LPC_LDRQ#/GPIO7	2	LPC_AD0/GPIO0
3	N.C.	4	LPC_AD1/GPIO1
5	SERIRQ/GPIO6	6	LPC_AD2/GPIO2
7	LPC_FRAME#/GPIO5	8	LPC_AD3/GPIO3
9	LPC_RST#	10	GND
11	BUF_LPC_CLK	12	GND
13	+3.3V_S	14	+3.3V_S

The LPC bus, used to manage the devices previously described in par. 3.3.15 and 3.3.17 is also carried out on a dual row, 14 pin, P2.54mm standard pin header, with the pinout shown in the table on the left.

Please remember that Qseven® specifications rel.2.0 share, on the same pins of the card edge connector, the LPC signals with eight general Purpose I/Os; this means that whatever interface is offered by the Qseven® module, it will be available on the pins of this pin header connector.

Please refer to the User Manual of the Qseven® module used for a description of effective signals available on this pin header, considering the correspondence with the card edge connector.

LPC_AD[0..4]/GPIO[0..1] LPC command/address/data signals, General purpose I/O [0..3].

BUF_LPC_CLK: LPC Clock Output line. Since there are many devices on LPC bus on CQ7-

A30 carrier board, this signal is not directly connected to the Qseven® card edge connector's signal LPC_CLK, but it comes out from a dedicated clock buffer. For this reason, on connector CN3 it is not possible to use this signal line as General Purpose I/O #4.

LPC_FRAME#, LPC Frame indicator, active low output line. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition. Pin multiplexed with General Purpose I/O #5.

SERIRQ: LPC Serialised IRQ request, bidirectional line. This signal is used only by peripherals requiring Interrupt support. It is shared with general Purpose I/O #6.

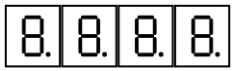
LPC_LDRQ#: LPC DMA request, active low input line. This signal is used only by peripherals requiring DMA or bus mastering. It is shared with General Purpose I/O #7

LPC_RST# signal is derived by PLT_RST# signal, by buffering it using a CMOS buffer.

3.3.19 POST Codes section

On x86 architectures, during the boot phase, usually the BIOS outputs on LPC bus some diagnostic progressive codes (a hexadecimal byte), which reflect the status of the last performed operation. This sequence (Power On Self Test, POST) is therefore useful for debugging purposes in case the Qseven® module fails to initialize properly. Indeed, in that case, the BIOS execution stops, and the last POST code transmitted is indicative of the point where the initialization failed.

For this reason on the CQ7-A30 board there are four seven-segment LCD display, which show the POST codes transmitted on ports 80h and 84h.



JP12 position	POST Codes addresses
1-2	80h / 84h
2-3	90h / 94h

The POST codes are usually transmitted on LPC bus at addresses 80h and 84, but could be available at addresses 90h and 94h. The selection of the address to be read is made using jumper JP12, which is a standard pin header, P2.54mm, 1x3 pin, according to the table on the left.

3.3.20 SPI Pin header

SPI Pin Header - CN7			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_S	2	+3.3V_S
3	SPI_CS0#	4	SPI_MOSI
5	SPI_CS1#	6	SPI_MISO
7	1-Wire_Bus	8	SPI_CLK
9	GND	10	GND

It is possible to use SPI interface, coming out from Qseven® card edge connector, for the connection of external SPI Devices (like EEPROM or Flash devices, but any kind of SPI device can be connected).

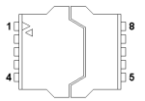
For this purpose, it is available a dual row, 10 pin, P2.54mm standard pin header, with the pinout shown in the table on the left.

On this pin header is also available the General Purpose 1-Wire signal. Please be aware, to avoid malfunctioning, that this signal is available only when JP5 jumper is set in position 1-2 (please check par.3.3.3)

3.3.21 SPI Flash socket

SPI Flash socket - CN6			
Pin	**Signal**	**Pin**	**Signal**
1	SPI_CS0#	8	+3.3V_S
2	SPI_MISO	7	SPI_HOLD#
3	SPI_WP#	6	SPI_CLK
4	GND	5	SPI_MOSI

For the cases when an external Flash is needed, on the carrier board it is provided an 8-pin SOIC socket for the housing of SPI Flashes.



Socket is type LOTES p/n ACA-SPI-004-K0 or equivalent, p. 1.27mm, with the pinout shown in the table on the left.

Almost all signals on this socket come directly from Qseven® Card Edge connector, with the following exceptions:

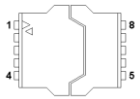
SPI_WP#: this signal is tied, through a 4k7Ω resistor, to +3.3V power rail. This means that when the Flash is powered, the protection from writing is automatically removed.

SPI_HOLD#: this signal too is tied, through a 4k7Ω resistor, to +3.3V_S power rail. This means that when the Flash is powered, the Hold condition of serial communication is automatically removed.

3.3.22 I2C EEPROM socket

I2C EEPROM socket - CN5			
Pin	**Signal**	**Pin**	**Signal**
1	A0	8	+3.3V_S
2	A1	7	WP
3	A2	6	GP0_I2C_CK
4	GND	5	GP0_I2C_DAT

In many applications it is useful to have a small non-volatile storage device, like an EEPROM.

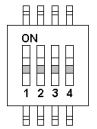


For this purpose, connected to I2C bus, there is an 8-pin SOIC socket type LOTES p/n ACA-SPI-004-K0 or equivalent, p. 1.27mm, with the pinout shown in the table on the left.

SW1 Switch	ON Position	OFF Position
1	WP = 0	WP = 1
2	A0 = 0	A0 = 1
3	A1 = 0	A1 = 1
4	A2 = 0	A2 = 1

Please notice that address lines (A0, A1 and A2) and Write Protect (WP) line have to be set manually set by the customer using a dedicated switch (SW1), which is placed right near the I2C EEPROM Socket.

Setting of these signals can be made according to the table on the left.



3.3.23 Pushbuttons

On the carrier board, there are four momentary pushbuttons (with contacts normally open) for the direct handling of Qseven® power management signals.

The first pushbutton, SW7, is placed on PWRBTN# signal. Upon the pressure of this pushbutton, the Qseven® module will perform a power up / power down sequence.

The second pushbutton, SW8, is placed on SLP_BTN# signal. Upon the pressure of this pushbutton, the Qseven® module will enter in a sleep state (is such states are supported).

The third pushbutton, SW9, is placed on RSTBTN# signal. Upon the pressure of this pushbutton, the Qseven® module will perform a reset.

The fourth pushbutton, SW10, is placed on LID_BTN# signal. Such a signal can be used by the Qseven® module to detect the opening / the closure of an external lid switch, like those used to detect opening / closure of the notebooks. Upon changes in LID_BTN# state, the OS could trigger the transition of the module from Working to Sleep status, or vice versa.

JP14 position	LID_BTN# status
Not Inserted	Normal working
Inserted	Tied to GND

It is possible to manage the LID_BTN# signal also using dedicated jumper JP14, which is a standard pin header, P2.54mm, 1x2 pin.

This same jumper can be used to manage an external, remote switch/pushbutton with contacts normally open.

3.3.24 Feature internal pin header

For further expandability of the system, on board there is an expansion connector, which carries out the signals related to Watch Dog, I2C bus, SM Bus, thermal and power management. These signals allow implementing, through external expansion modules, further functionalities that are not already realised by the carrier board.

Feature pin header - CN4

Pin	Signal	Pin	Signal
1	+5V_S	2	+5V_A
3	+3.3V_S	4	HDD_ACT#
5	GP0_I2C_DAT	6	SMB_CLK
7	GP0_I2C_CLK	8	SMB_DAT
9	N.C.	10	GP_PWM_OUT0
11	N.C.	12	GP_PWM_OUT1
13	PSON#	14	GP_PWM_OUT2
15	SUS_S3#	16	1-Wire_Bus
17	GND	18	GND
19	THRMTRIP#	20	SMB_ALERT#
21	N.C.	22	N.C.
23	SUS_STAT#	24	GP_TIMER_IN
25	N.C.	26	SUS_S5#
27	WDTRIG#	28	THRM#
29	WDOUT	30	N.C.
31	BATLOW#	32	WAKE#
33	LVDS_DID_DAT	34	N.C.
35	LVDS_DID_CLK	36	RSTBTN#
37	GND	38	GND
39	PWRBTN#	40	PWGIN

For this purpose, it is available a dual row, 40 pin, P2.54mm standard pin header, with the pinout shown in the table on the left.

HDD_ACT#: Disk drive activity signal, active low. It is derived as the logical AND of SDIO_ACT# and SATA_ACT# signals.

PSON#: this signal (+5V_A electrical level) is derived by inverting SUS_S3# signal.

The signals not described until now come out directly from the Qseven® connector; please check the related table for a description of them.

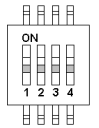
A special consideration has to be made on signal GP_PWM_OUT[0..2] and GP_TIMER_IN.

These, indeed, are multiplexed signals available on Qseven® card edge connector, which can be used, respectively, also as LVDS_BLT_CTRL, FAN_PWMOUT, SPKR and FAN_TACHOIN.

By using the dedicated Dip Switch SW11, it is possible to select individually if these signals must have the specific or the General Purpose functionality.

SW11 Switch	ON Position	OFF Position
1	LVDS_BLT_CTRL	GP_PWM_OUT0
2	FAN_PWMOUT	GP_PWM_OUT1
3	SPKR	GP_PWM_OUT2
4	FAN_TACHOIN	GP_TIMER_IN

Setting of these signals can be made according to the table on the left.

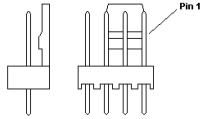


3.3.25 FAN Connectors

The CQ7-A30 carrier board makes available two dedicated connectors for external tachometric 3- or 4-wire FANs.

FAN Connector #0 - CN37	
Pin	**Signal**
1	GND
2	FAN_POWER_0
3	FAN_TACHO_IN_0
4	FAN_CTRL_0

The first connector, CN37, is a 4-pin single line TH connector, type MOLEX 47053-3000 or equivalent, with the pinout shown in the table on the left.



Mating connector MOLEX 47054-1000 receptacle with MOLEX 2759 KK® crimp terminals.

FAN_POWER_0: power rail for FAN #0. The voltage of this power rail is set using the jumper JP15, which is a standard pin header, P2.54mm, 1x3 pin, according to the table below.

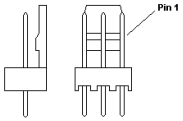
FAN_TACHO_IN_0: tachometric input from the connected fan.

FAN_CTRL_0: PWM control for the connected fan, +5V_S electrical level. This signal is derived directly from Qseven® signal FAN_PWMOUT.

JP15 position	FAN_POWER_0 voltage
1-2	+12V_S
2-3	+5V_S

FAN Connector #1 - CN38	
Pin	**Signal**
1	GND
2	FAN_POWER_1
3	FAN_TACHO_IN_1

The second FAN Connector, CN38, is a 3-pin single line TH connector, type MOLEX 22-27-2031 or equivalent, with pinout shown in the table on the left.



Mating connector: MOLEX 22-01-2035 receptacle with MOLEX 2759 or 4809 KK® crimp terminals.

FAN_TACHO_IN_1: tachometric input from the connected fan.

JP16 position	FAN_POWER_1 voltage
1-2	+12V_S
2-3	+5V_S

FAN_POWER_1: power rail for FAN#1. The voltage of this power rail can set using the jumper JP16, which is a standard pin header, P2.54mm, 1x3 pin, according to the table on the left.

JP17 position	FAN_POWER_1 PWM control
Not Inserted	Enabled
Inserted	Disabled (fixed voltage)

It is also possible to disable the PWM control of FAN_POWER_1, by using jumper JP17

3.3.26 Manufacturer and Debug Connectors

According to Qseven® specifications, on MXM connector there are some pins that are reserved for manufacturing and debugging purposes (MFG_NC0÷MFG_NC4). These signals are reserved to the manufacturer of the Qseven CPU module, so it is not recommended to use them. Anyway they can be accessed through two different connectors.

MFG_NCx signals can be used, by the Qseven® module, as a JTAG port or Debug UART. Please refer to the User manual of the Qseven® module for information about the proper assignment of JTAG / UART signals to the MFG_NCx signals (although the assignment shall correspond to that defined by the Qseven® specifications).

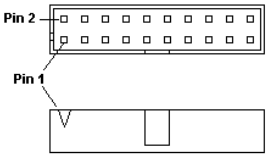
JP20 position	MFG_NC2 routed to
1-2	JTAG connector CN41 (JTAG_TDI)
2-3	Debug USB port CN42 (DEBUG_RX)

JP21 position	MFG_NC1 routed to
1-2	JTAG connector CN41 (JTAG_TDO)
2-3	Debug USB port CN42 (DEBUG_TX)

Moreover, debug UART signals (available on MFG_NC1 and MFG_NC2 pins of Qseven® card edge connector), can be routed to a standard connector or to an USB-to-UART bridge, which will allow the implementation of a debug USB port. Selection is made using jumpers JP20 and JP21, according to the tables on the left.

MFG connector - CN41			
Pin	Signal	Pin	Signal
1	+3.3V_A	2	N.C.
3	MFG_NC4 (see JP25)	4	GND
5	MFG_NC2 (see JP20)	6	GND
7	MFG_NC3	8	GND
9	MFG_NC0	10	GND
11	10kΩ pull-down to GND	12	GND
13	MFG_NC1 (see JP21)	14	GND
15	SRST#	16	GND
17	N.C.	18	GND
19	N.C.	20	GND

When both JP20 and JP21 are set in position 1-2, then all MFG signals are available on the MFG connector, CN41, which is a 2.54mm pitch connector, type MOLEX p/n 70246-2004 or equivalent.



Mating connector: MOLEX 22-55-2202 receptacle with MOLEX 70058 or 71851 crimp terminals.

Please be aware that Debug UART, when routed to this connector (on pins dedicated to signals MFG_NC1 and MFG_NC2) will be available at TTL level, i.e. it cannot be used for a direct connection to a common RS-232 serial port (like those available on PCs).

Regarding MFG_NC4 signal, a dedicated 2-way jumper, JP25, allows selecting if this signal must be connected to pin #3 of CN41 or not (it could be routed to pin 15, see jumper JP24).

JP25 position	MFG_NC4 connection on CN41 pin #3
Not Inserted	Disconnected
Inserted	Connected

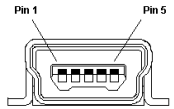
JP24 position	SRST# connected to
1-2	RSTBTN# signal
2-3	MFG_NC4 signal

SRST# signal (pin 15 of connector CN41) can have two different routings, depending on the settings of jumper JP24

JP18 position	MFG_NC3 pull-up / pull-down
1-2	10kΩ pull-up to +3.3V_S
2-3	10kΩ pull-down

Two other 3-way jumpers can be used to place a pull-up or pull-down resistor on signals MFG_NC3 and MFG_NC4.

JP19 position	MFG_NC4 pull-up / pull-down
1-2	10kΩ pull-up to +3.3V_S
2-3	10kΩ pull-down



When MFG_NC1 and MFG_NC2 signals are not routed to connector CN41 (i.e., jumpers JP20 and JP21 are set to position 2-3), then it is possible to have a debug USB port on mini-B USB connector CN42

This debug USB port is realised converting the Debug UART signals to USB by using a Silicon Labs® CP2104 USB-to-UART bridge.

By using Silicon Labs® VCP drivers on the PC connected to this USB port (drivers available at http://www.silabs.com/products/interface/usbtouart/Pages/usb-to-uart-bridge.aspx), the debug USB port will be exploitable by any COM port application, exactly like if it were a standard serial port. Please remember that Qseven® module will have to work in device (i.e. client) mode.

Chapter 4.
Development Kit Accessories

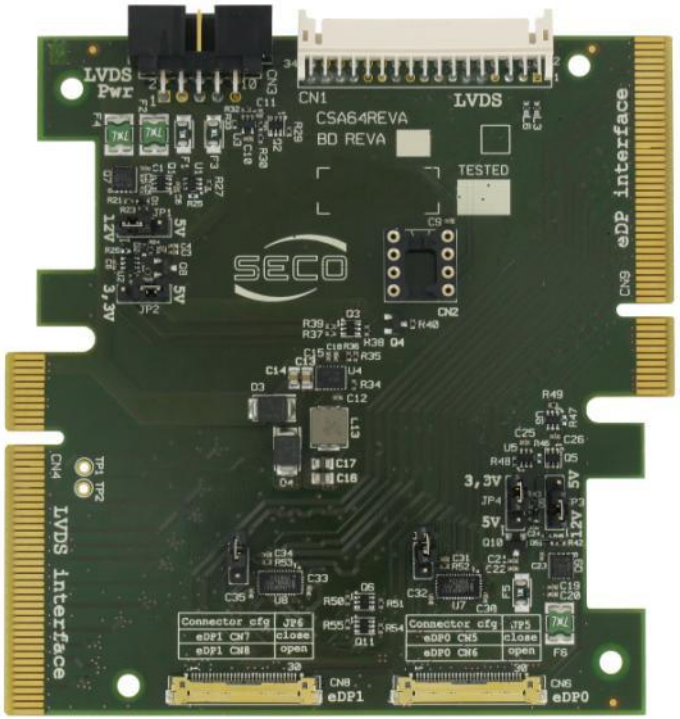
- LVDS/eDP Adapter Module VA64
- DP++/HDMI Adapter Module VA65
- Accessories Kit

4.1 LVDS/eDP Adapter Module VA64

The CQ7-A30 Carrier board doesn't offer any LVDS or eDP connector for the direct connection of external displays to these interfaces, which could come out from the Qseven® module plugged in in CN1 connector. These interfaces, instead, are carried out to the generic PCI-e x8-type slot CN20.

In order to connect any external display to one of these interfaces (LVDS or eDP, depending on the interface offered by the Qseven® module used), in the Development Kit it is available an LVDS/eDP Adapter module, code VA64, which can be observed in the following pictures.

VA64 TOP SIDE



VA64 BOTTOM SIDE

It is possible to see that this adapter module has two different edge connectors, named CN4 and CN9, which allow the insertion of the adapter module in the card edge connector CN20 in two different ways.

If the module is plugged in CN20 slot using the CN4 edge connector (marked with the writing "LVDS interface"), then the signals coming from the CQ7-A30 carrier board will be carried to connectors CN1 and CN3, and will be usable for the connection of LVDS displays.

On the other side, if the VA64 module is plugged in the carrier's CN20 slot using the CN9 edge connector (marked with the writing "eDP interface"), then the signals coming from the CQ7-A30 carrier board will be carried to connectors CN5, CN6, CN7 and CN3, and will be usable for the connection of eDP displays.

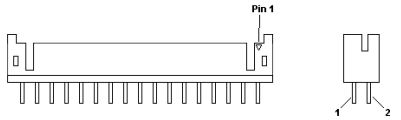
4.1.1 LVDS working mode

If the Qseven® module used with CQ7-A30 carrier board offers an LVDS interface, then it is necessary to plug the adapter module in LVDS/eDP slot using the adapter's dedicated edge connector CN4.

In this case, only the module's connectors CN1, CN2 and CN3 will be usable.

LVDS connector - CN1

Pin	Signal	Pin	Signal
2	LVDS_DID_DAT	1	LVDS_DID_CLK
4	N.C.	3	N.C.
6	GND	5	LVDS_A0-
8	LVDS_A0+	7	LVDS_VDD_EN
10	LVDS_A1-	9	LVDS_A1+
12	LVDS_BACKLIGHT_EN	11	LVDS_A2+
14	LVDS_A2-	13	N.C.
16	LVDS_A_CLK-	15	LVDS_A_CLK+
18	LVDS_BLT_CTRL	17	LVDS_A3+
20	LVDS_A3-	19	GND
22	LVDS_B0-	21	LVDS_B0+
24	GND	23	LVDS_B1-
26	LVDS_B1+	25	GND
28	LVDS_B2-	27	LVDS_B2+
30	GND	29	LVDS_B_CLK+
32	LVDS_B_CLK-	31	N.C.
34	LVDS_B3+	33	LVDS_B3-



For the connection, a connector type JST S34B-PHDSS or equivalent (2 x 17p, male, right angle, P2, low profile, polarised) is provided, with the pin-out shown in the table on the left. Mating connector: JST p/n PHDR-34VS with HR SPHD-002T-P0.5 female crimp terminals.

Display Data Channel signals are also provided, in case that the Qseven® module used supports them.

Most of the signals available on this connector come out directly from the Qseven® connector; please check the related table for a description of the signals.

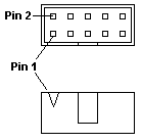
LVDS_BACKLIGHT_EN is the signal used for Backlight enabling, is the logical conjunction (i.e. AND) of the signal LVDS_BLEN and the signal PLT_RST#.

LVDS_VDD_EN is the signal used for LCD enabling, is the logical conjunction (i.e. AND) of the signal LVDS_PPEN and the signal PLT_RST#.

These operations on signals LVDS_BACKLIGHT_EN and LVDS_VDD_EN have been done so that at each reset of the module, the eventually connected backlight and display will also turn off themselves.

Backlight and LCD PSU connector - CN3			
Pin	Signal	Pin	Signal
1	LVDS_SW_VDD_FUSE	2	LVDS_SW_BACK_FUSE
3	+5V_S (Fuse protected)	4	+12V_S (Fuse protected)
5	LVDS_VDD_EN	6	LVDS_BACKLIGHT_EN
7	Analogic Dimming	8	LVDS_BLT_CTRL
9	GND	10	GND

There is also dedicated connector for backlight / LCD PSU connector.



The connector, CN3, is an IDC connector, dual row, 10 pin, p2.54 mm connector, type MOLEX p/n 70246-1004 or equivalent.

Mating connector: MOLEX p/n 22-25-2102 with 70058 series female crimp terminals.

LVDS_SW_VDD_FUSE and LVDS_SW_BACK_FUSE mean Switched_VDD and Switched_Backlight, i.e., these are the voltages that can be supplied to LCD and backlight, respectively, and are enabled/disabled via the signals LVDS-PPEN and LVDS_BLEN, respectively.

The suffix _FUSE means that these voltages are protected by a polyswitch resettable fuse.

Analogic_Dimming is a +5V signal, derived from the PWM signal LVDS_BLT_CTRL coming from Qseven® module, for direct analogic control of backlights not supporting PWM.

JP2 position	LVDS_SW_VDD_FUSE Voltage
1-2	+5V_{LVDS}
2-3	+3.3V_{LVDS}

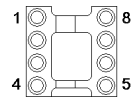
LCD software-driven voltage, i.e. signal LVDS_SW_VDD_FUSE, can also be regulated to be connected to +5V_{LVDS} or +3.3V_{LVDS}, using module's jumper JP2, which is a standard pin header, P2.54mm, 1x3 pin.

JP1 position	LVDS_SW_BACK_FUSE Voltage
1-2	+12V_{LVDS}
2-3	+5V_{LVDS}

Similarly, backlight software-driven voltage, signal LVDS_SW_BACK_FUSE, can be regulated to be connected to +12V_{LVDS} or +5V_{LVDS}, using module's jumper JP1, which is another standard pin header, P2.54mm, 1x3 pin.

LVDS EEPROM socket - CN2			
Pin	Signal	Pin	Signal
1	GND	8	+3.3V_S
2	GND	7	GND
3	GND	6	LVDS_DID_CK
4	GND	5	LVDS_DID_DAT

It could be possible that the TFT panel used on LVDS connection is not able to communicate to the Qseven® module its parameters for correct synchronisation/configuration, or that it is necessary to use peculiar timing parameters.



In both these cases, it is possible to use a specific I2C EEPROM programmed with correct timing data.

For this purpose, an 8-pin DIP socket p2.54mm, type TE p/n 2-1571552-2 or equivalent is provided, with the pinout shown in the table on the left:

4.1.2 eDP working mode

If the Qseven® module used with CQ7-A30 carrier board offers support for eDP displays (up to two interfaces), then it is necessary to plug the adapter module in LVDS/eDP slot using the adapter's dedicated edge connector CN9.

In this case, only the module's connectors CN5, CN6, CN7 and CN8 will be usable.

Moreover, it is possible to use two separated 30-pins or 40-pins connectors for the connection of the eDP displays. All the connectors are VESA® certified connectors for Display Port interface.

JP5 position	eDP0 interface available on:
Inserted	40-pin connector CN5
Not Inserted	30-pin connector CN6

JP6 position	eDP1 interface available on:
Inserted	40-pin connector CN7
Not Inserted	30-pin connector CN8

Selection of the suitable connector for each eDP interface is made using jumpers JP5 and JP6, which are two standard pin header, P2.54mm, 1x2 pin.

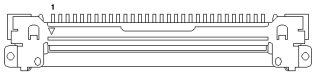
JP4 position	eDP_SW_VDD_FUSE Voltage
1-2	$+5V_{eDP}$
2-3	$+3.3V_{eDP}$

LCD software-driven voltage, i.e. signal eDP_SW_VDD_FUSE, can also be regulated to be connected to $+5V_{eDP}$ or $+3.3V_{eDP}$, using module's jumper JP4, which is a standard pin header, P2.54mm, 1x3 pin.

JP3 position	eDP_SW_BACK_FUSE Voltage
1-2	$+12V_{eDP}$
2-3	$+5V_{eDP}$

Similarly, backlight software-driven voltage, signal eDP_SW_BACK_FUSE, can be regulated to be connected to $+12V_{eDP}$ or $+5V_{eDP}$, using module's jumper JP3, which is another standard pin header, P2.54mm, 1x3 pin.

When using 30-pin eDP connectors (for eDP interface #0 and/or #1), placed on top side of the module, the connector used is type STARCONN p/n 300E30-0010RA-G3.



eDP_BACKLIGHT_EN is the signal used for Backlight enabling, is the logical conjunction (i.e. AND) of the signal eDP_BLEN (LVDS_BLEN on CQ7-A30 carrier board's connector CN20) and the signal PLT_RST#. This has been done so that at each reset of the module, the eventually connected backlight and display will also turn off themselves.

30-pin eDP #0 connector CN6		30-pin eDP #1 connector CN8	
Pin nr.	Pin name	Pin nr.	Pin name
1	N.C.	1	N.C.
2	eDP_SW_BACK_FUSE	2	eDP_SW_BACK_FUSE
3	eDP_SW_BACK_FUSE	3	eDP_SW_BACK_FUSE
4	eDP_SW_BACK_FUSE	4	eDP_SW_BACK_FUSE
5	eDP_SW_BACK_FUSE	5	eDP_SW_BACK_FUSE
6	N.C.	6	N.C.
7	N.C.	7	N.C.
8	LVDS_BLT_CTRL	8	LVDS_BLT_CTRL
9	eDP_BACKLIGHT_EN	9	eDP_BACKLIGHT_EN
10	GND	10	GND
11	GND	11	GND
12	GND	12	GND
13	GND	13	GND
14	eDP0_HPD	14	eDP1_HPD
15	GND	15	GND
16	GND	16	GND
17	N.C.	17	N.C.
18	eDP_SW_VDD_FUSE	18	eDP_SW_VDD_FUSE
19	eDP_SW_VDD_FUSE	19	eDP_SW_VDD_FUSE
20	GND	20	GND
21	eDP0_AUX-	21	eDP1_AUX-
22	eDP0_AUX+	22	eDP1_AUX+
23	GND	23	GND
24	eDP0_TX0+	24	eDP1_TX0+
25	eDP0_TX0-	25	eDP1_TX0-
26	GND	26	GND
27	eDP0_TX1+	27	eDP1_TX1+
28	eDP0_TX1-	28	eDP1_TX1-
29	GND	29	GND
30	N.C.	30	N.C.

When using 40-pin eDP connectors (for eDP interface #0 and/or #1), placed on top side of the module, the connector used is type IS-NEW p/n CR10-S40R1-2, a 40-poles 0.5mm pitch FPC connector.

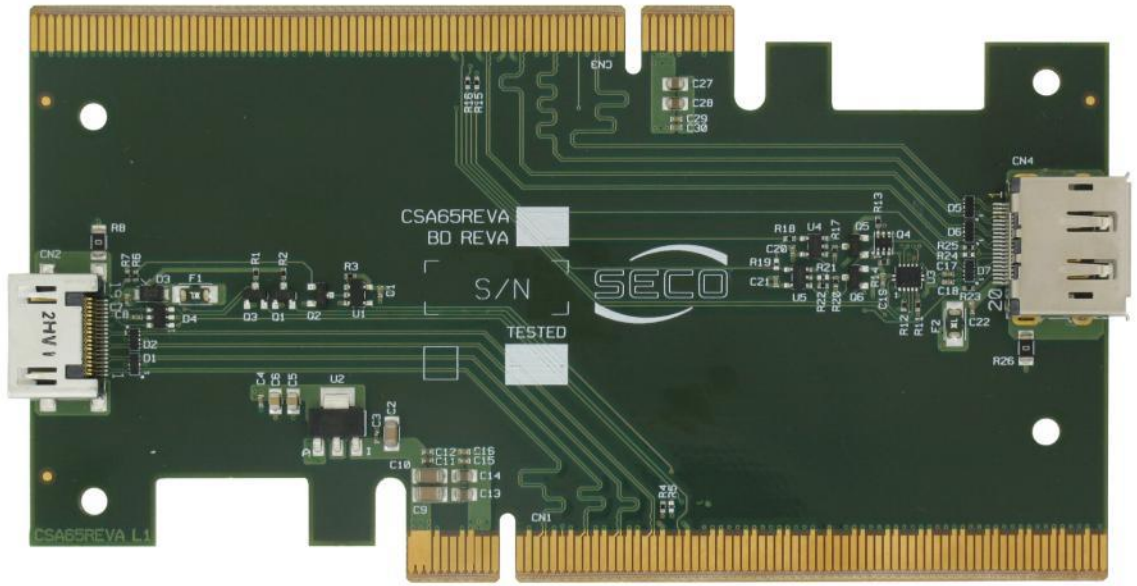
40-pin eDP #0 connector CN5		40-pin eDP #1 connector CN7	
Pin nr.	Pin name	Pin nr.	Pin name
1	N.C.	1	N.C.
2	eDP_SW_BACK_FUSE	2	eDP_SW_BACK_FUSE
3	eDP_SW_BACK_FUSE	3	eDP_SW_BACK_FUSE
4	eDP_SW_BACK_FUSE	4	eDP_SW_BACK_FUSE
5	eDP_SW_BACK_FUSE	5	eDP_SW_BACK_FUSE
6	N.C.	6	N.C.
7	N.C.	7	N.C.
8	LVDS_BLT_CTRL	8	LVDS_BLT_CTRL
9	eDP_BACKLIGHT_EN	9	eDP_BACKLIGHT_EN
10	GND	10	GND
11	GND	11	GND
12	GND	12	GND
13	GND	13	GND
14	eDP0_HPD	14	eDP0_HPD
15	GND	15	GND
16	GND	16	GND
17	N.C.	17	N.C.
18	GND	18	GND
19	N.C.	19	N.C.
20	eDP_SW_VDD_FUSE	20	eDP_SW_VDD_FUSE
21	eDP_SW_VDD_FUSE	21	eDP_SW_VDD_FUSE
22	eDP_SW_VDD_FUSE	22	eDP_SW_VDD_FUSE
23	eDP_SW_VDD_FUSE	23	eDP_SW_VDD_FUSE
24	GND	24	GND
25	eDP0_AUX-	25	eDP0_AUX-
26	eDP0_AUX+	26	eDP0_AUX+
27	GND	27	GND
28	eDP0_TX0+	28	eDP0_TX0+

29	eDP0_TX0-	29	eDP0_TX0-
30	GND	30	GND
31	eDP0_TX1+	31	eDP0_TX1+
32	eDP0_TX1-	32	eDP0_TX1-
33	GND	33	GND
34	eDP0_TX2+	34	eDP0_TX2+
35	eDP0_TX2-	35	eDP0_TX2-
36	GND	36	GND
37	eDP0_TX3+	37	eDP0_TX3+
38	eDP0_TX3-	38	eDP0_TX3-
39	GND	39	GND
40	N.C.	40	N.C.

4.2 DP++/HDMI Adapter Module VA65

The CQ7-A30 Carrier board doesn't offer any HDMI or DP connector for the direct connection of external displays to these interfaces, which could come out from the Qseven® module plugged in in CN1 connector. These interfaces, instead, are carried out to the generic PCI-e x16-type slot CN19.

In order to connect any external display to one of these interfaces (HDMI or DP, depending on the interface offered by the Qseven® module used), in the Development Kit it is available a DP++/HDMI Adapter module, code VA65, which can be observed in the following picture.



It is possible to see that this adapter module has two different edge connectors, named CN1 and CN3, which allow the insertion of the adapter module in the card edge connector CN19 in two different ways.

If the module is plugged in CN19 slot using the CN1 edge connector, then the signals coming from the CQ7-A30 carrier board will be carried to connectors CN2, and will be usable for the connection of HDMI displays.

On the other side, if the VA65 module is plugged in the carrier's CN19 slot using the CN3 edge connector, then the signals coming from the CQ7-A30 carrier board will be carried to connector CN4, and will be usable for the connection of DP displays. In case the Qseven® module used supports multimode Display Port (DP++) interface, it is possible to connect HDMI or DVI displays to connector CN4 by using an adapter.

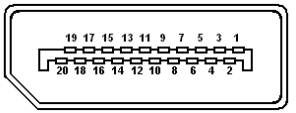
> **!** Please be aware that HDMI connection on connector CN2 is possible only if the Qseven® module used supports HDMI directly (i.e., it doesn't require the level shifters on the carrier board / adapter card). If HDMI is not directly supported, please plug the VA65 DP++/HDMI adapter module using the card edge connector CN4.

4.2.1 DP++ working mode

If the Qseven® module used with CQ7-A30 carrier board offers support for DP/DP++ displays, then it is necessary to plug the adapter module in DP++/HDMI slot using the adapter's dedicated edge connector CN3.

DP++ connector - CN4			
Pin	**Signal**	**Pin**	**Signal**
1	DP_LANE0+	2	GND
3	DP_LANE0-	4	DP_LANE1+
5	GND	6	DP_LANE1-
7	DP_LANE2+	8	GND
9	DP_LANE2-	10	DP_LANE3+
11	GND	12	DP_LANE3-
13	CAD	14	HDMI_CEC
15	HDMI_CTRL_CLK / DP_AUX+	16	GND
17	HDMI_CTRL_DAT / DP_AUX-	18	DP_HPD
19	GND	20	+3.3V_{DP}

In this case, only the module's connector CN4 will be usable, which is a standard DP connector, type WinWin p/n WDPE-20F3L1BU3 or equivalent, with the pinout shown in the table on the left.



Such a pinout allows the implementation of a DP++ interface, i.e. an interface able to support both DP and HDMI/DVI displays (by using dedicated adapters). Please remember that this feature is possible only in the case the Qseven® module used supports it.

In case that DP++ is supported, when a DP cable is connected, then this interface will recognize it, and on pins 15/17 there will be the Display Port Auxiliary channel signals. Instead, when a DP-to-HDMI adapter is mounted, it will drive opportunely the CAD signal, which will make available HDMI_CTRL_CLK and HDMI_CTRL_DAT signals on the same pins.

Further signals involved in DP management are the following (please check the Qseven® connector's description table for a correspondence between DP lanes and TMDS lanes):

DP_LANE0+/DP_LANE0-: Display Port differential pair #0.

DP_LANE1+/DP_LANE1-: Display Port differential pair #1.

DP_LANE2+/DP_LANE2-: Display Port differential pair #2.

DP_LANE3+/DP_LANE3-: Display Port differential pair #3.

DP_HPD: Hot Plug Detect Input signal.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. This signal is used only for HDMI compatibility when a HDMI adapter is connected to the DP connector. According to Qseven® specifications, the signal is, in reality, a General Purpose 1_wire bus interface, that can be used for implementation of HDMI_CEC. In case the Qseven® module used doesn't support the HDMI_CEC functionality, then this signal could be not available or have a different utilisation. Furthermore, this signal will be available on the DP++/HDMI card edge connector only in case that jumper JP5 on the carrier board is placed in position 2-3 (please check par. 3.3.3). Please refer to the User Guide of the Qseven® module used for more information on the allowed uses of this signal.

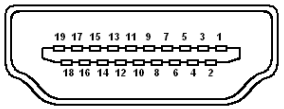
For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

4.2.2 HDMI working mode

If the Qseven® module used with CQ7-A30 carrier board offers direct support for HDMI displays, then it is necessary to plug the adapter module VA65 in DP++/HDMI slot using the adapter's dedicated edge connector CN1.

HDMI connector - CN2			
Pin	**Signal**	**Pin**	**Signal**
1	TMDS_LANE2+	2	GND
3	TMDS_LANE2-	4	TMDS_LANE1+
5	GND	6	TMDS_LANE1-
7	TMDS_LANE0+	8	GND
9	TMDS_LANE0-	10	TMDS_CLK+
11	GND	12	TMDS_CLK-
13	HDMI_CEC	14	---
15	HDMI_CTRL_CLK	16	HDMI_CTRL_DAT
17	GND	18	$+5V_{HDMI}$
19	HDMI_HPD		

In this case, only the module's connector CN2 will be usable, which is a standard certified HDMI connector, type A, model HIROSE p/n MD60-19P, with the pinout shown in the table on the left.



Signals involved in HDMI management are the following:

TMDS_CLK+/TMDS_CLK-: TMDS differential Clock.

TMDS_LANE0+/TMDS_LANE0-: TMDS differential pair #0.

TMDS_LANE1+/TMDS_LANE1-: TMDS differential pair #1.

TMDS_LANE2+/TMDS_LANE2-: TMDS differential pair #2.

HDMI_CTRL_DAT: DDC Data line for HDMI panel.

HDMI_CTRL_CLK: DDC Clock line for HDMI panel.

HDMI_CEC: HDMI Consumer Electronics Control (CEC) Line. As already described in the description of DP++ connector CN4, this signal is, in reality, a General Purpose 1_wire bus interface, that can be used for implementation of HDMI_CEC functionality. The support of such functionality depends on the Qseven® module used. Furthermore, this signal will be available on the DP++/HDMI card edge connector only in case that jumper JP5 on the carrier board is placed in position 2-3.

HDMI_HPD: Hot Plug Detect Input signal.

For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

Always use HDMI-certified cables for the connection between the board and the HDMI display; a category 2 (High-Speed) cable is recommended for higher resolutions, category 1 cables can be used for 720p resolution.

4.3 Accessories Kit

In the Development Kit are also included some items that can be useful for the most common operations with the Development Kit

This accessories kit includes the following items

- 12V 80W Notebook Power Adapter
- Power Cord for the Notebook Power Adapter, with US NEMA 5-15P plug termination for direct use in the Americas and Japan
- USA NEMA 5-15R to European CEE7/7 Plug Adapter (for use in area Europe, Indonesia, Korea)
- USA NEMA 5-15R to UK BS1363 Plug Adapter (for use in area England, Hong Kong, U.A.E., Singapore, Malaysia)
- 4-wire Power cable, for the adapting of other external PSUs to Power In connector CN30
- HDMI video cable
- DP video cable
- DP++ to HDMI adapter (dongle)
- Dual USB 2.0 Type A adapters with standard PC mounting plate. Can be used to carry out the signals of internal USB ports #6-#7 (connector CN32) to standard USB 2.0 Type A receptacles
- SATA 7p data cable
- SATA power cable, for connection of power rails of external SATA disks / SSDs to internal SATA power connector CN10
- SATA 7+15p data + power cable, for the connection of external SATA disks / SSDs to internal SATA connector CN9

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